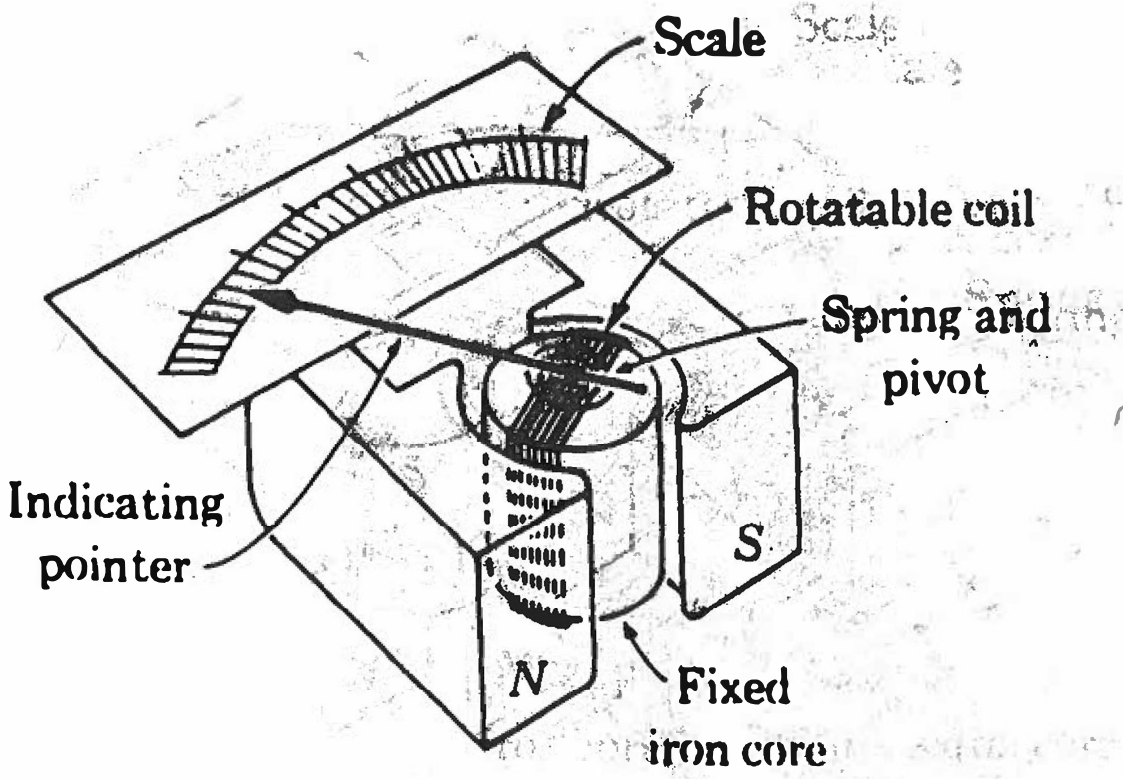
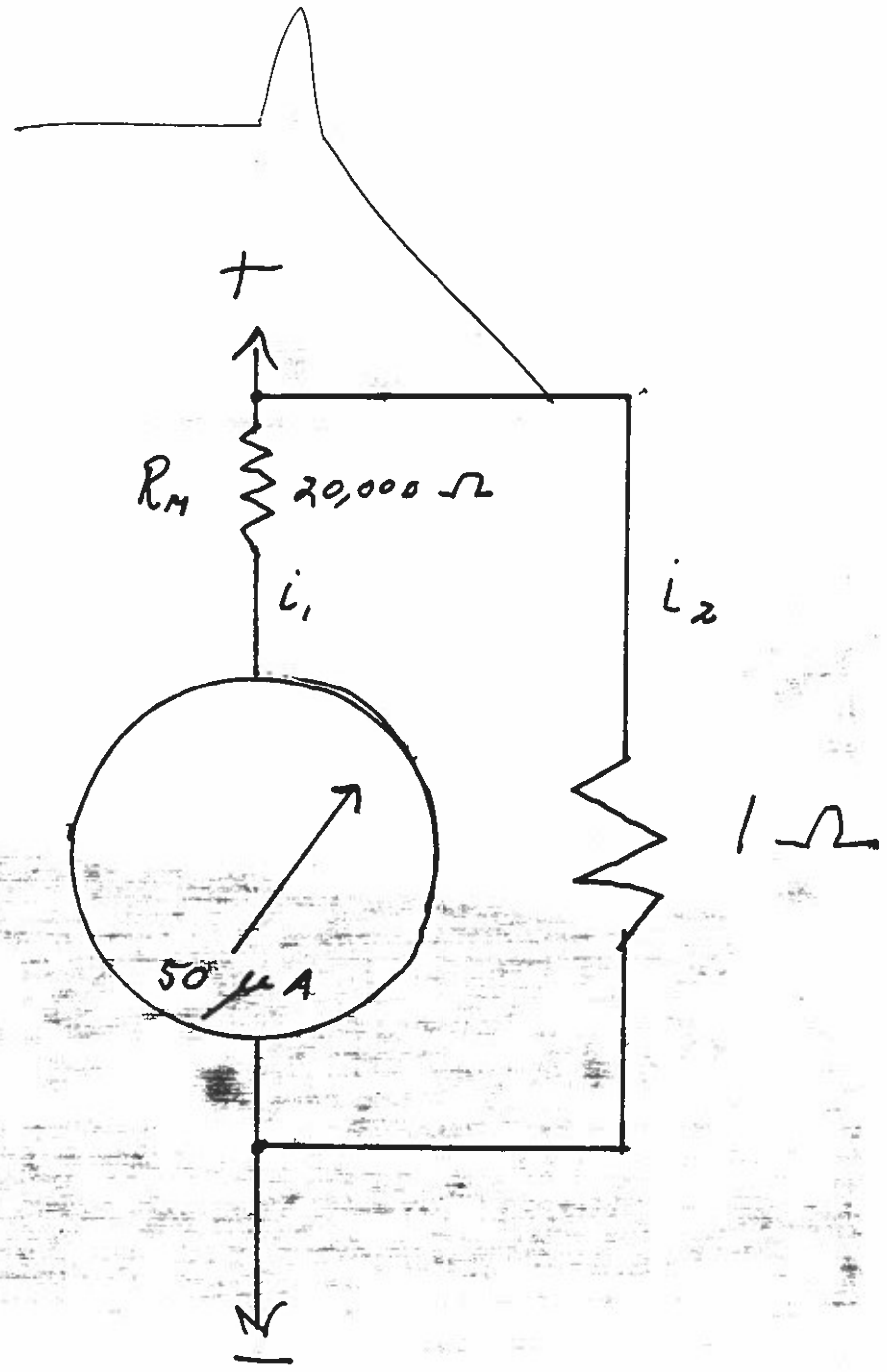
EXP # 1 - BASIC ELECTRICAL MEASUREMENTS



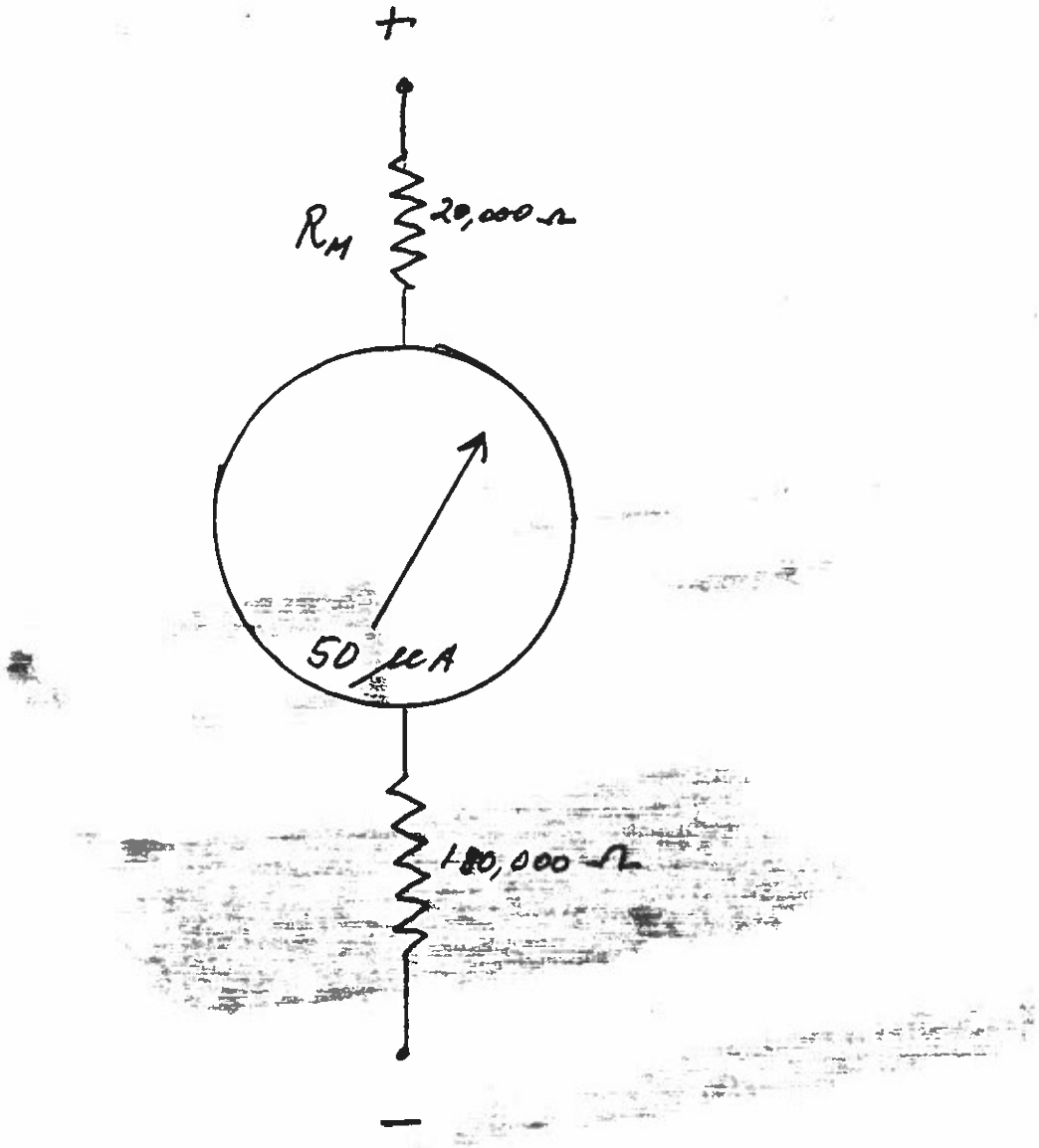
D'Arsonval movement

1/15/92



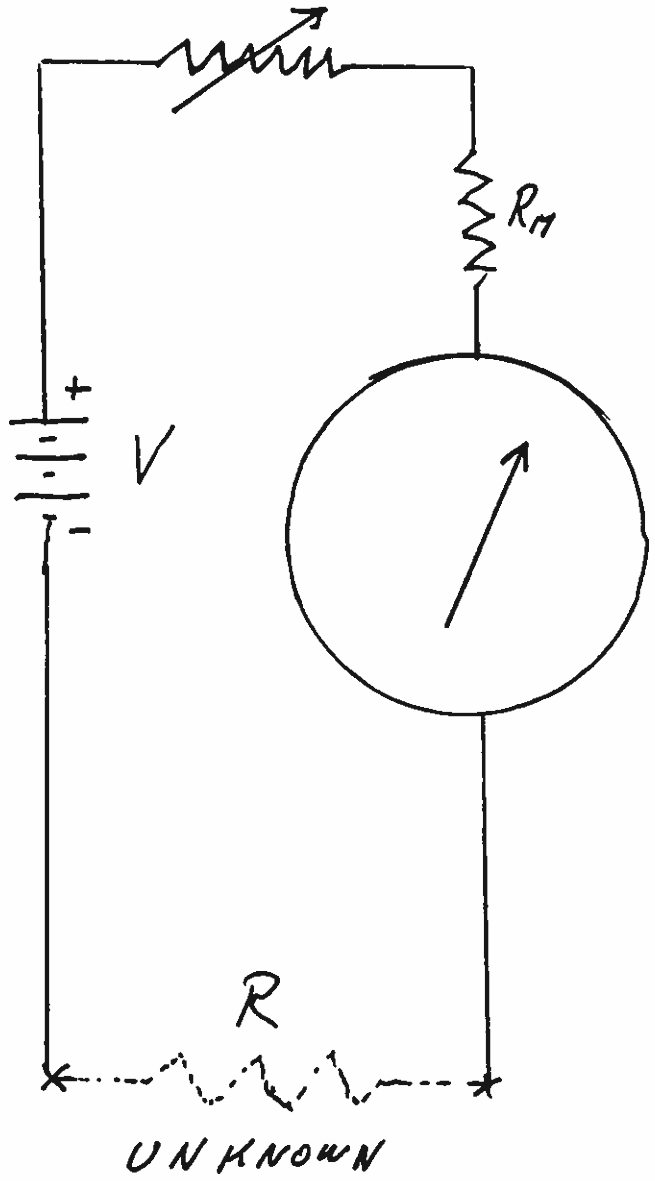
AMMETER

1 AMP FULL SCALE

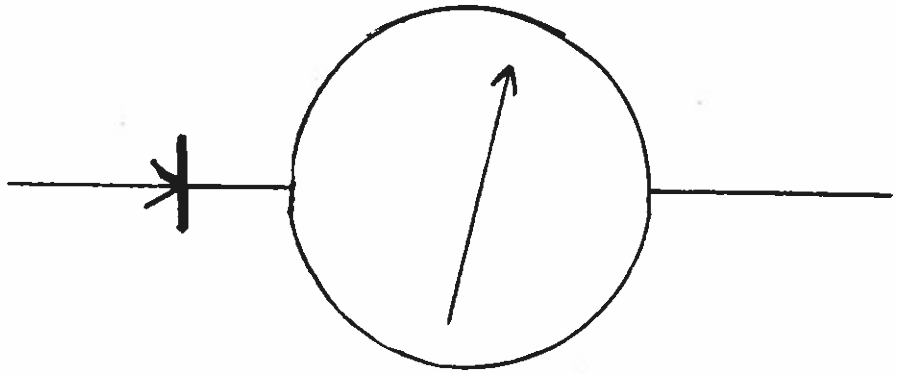


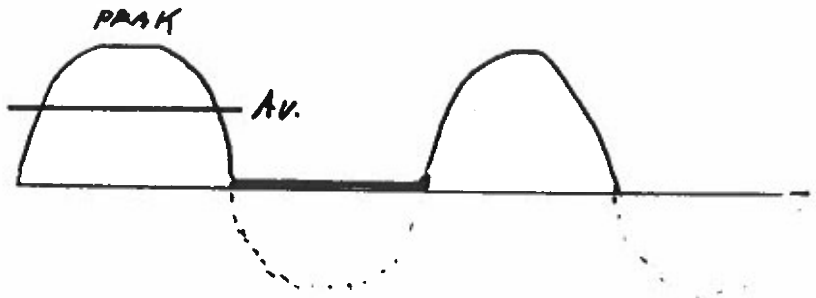
VOLTMETER

10 VOLTS FULL SCALE



OHMMETER





$$V_{AV.} = \frac{\omega}{\pi} \int_0^{\frac{\pi}{\omega}} V \sin(\omega t)\, dt$$

$$= \frac{2}{\pi} = .637\, V_{PEAK}$$

ALTERNATING VOLTAGE

AVERAGE MEASUREMENT

POWER IS A FUNCTION OF

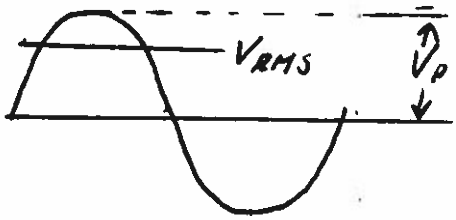
VOLTAGE SQUARED

$$P = W = \frac{V^2}{R} = I^2 R$$

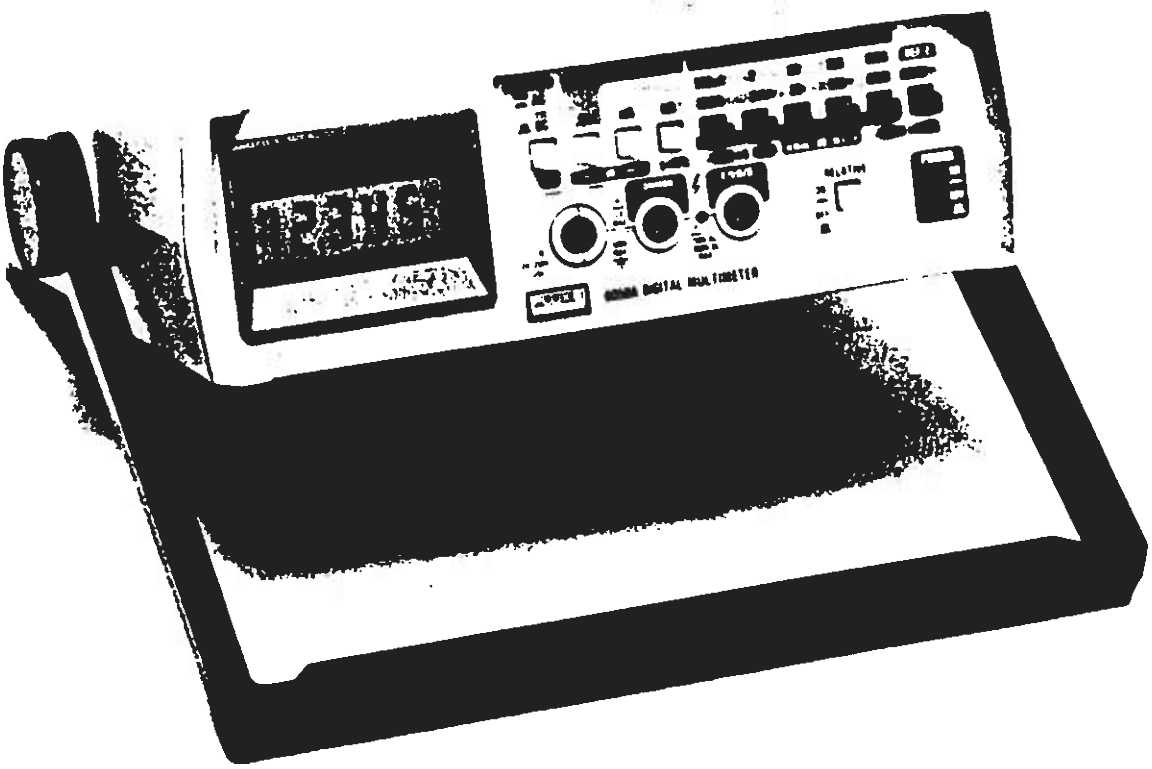
$$\therefore V_{RMS} = \left[\frac{1}{T} \int_0^T v^2(t)\, dt \right]^{1/2}$$

FOR SINE WAVE

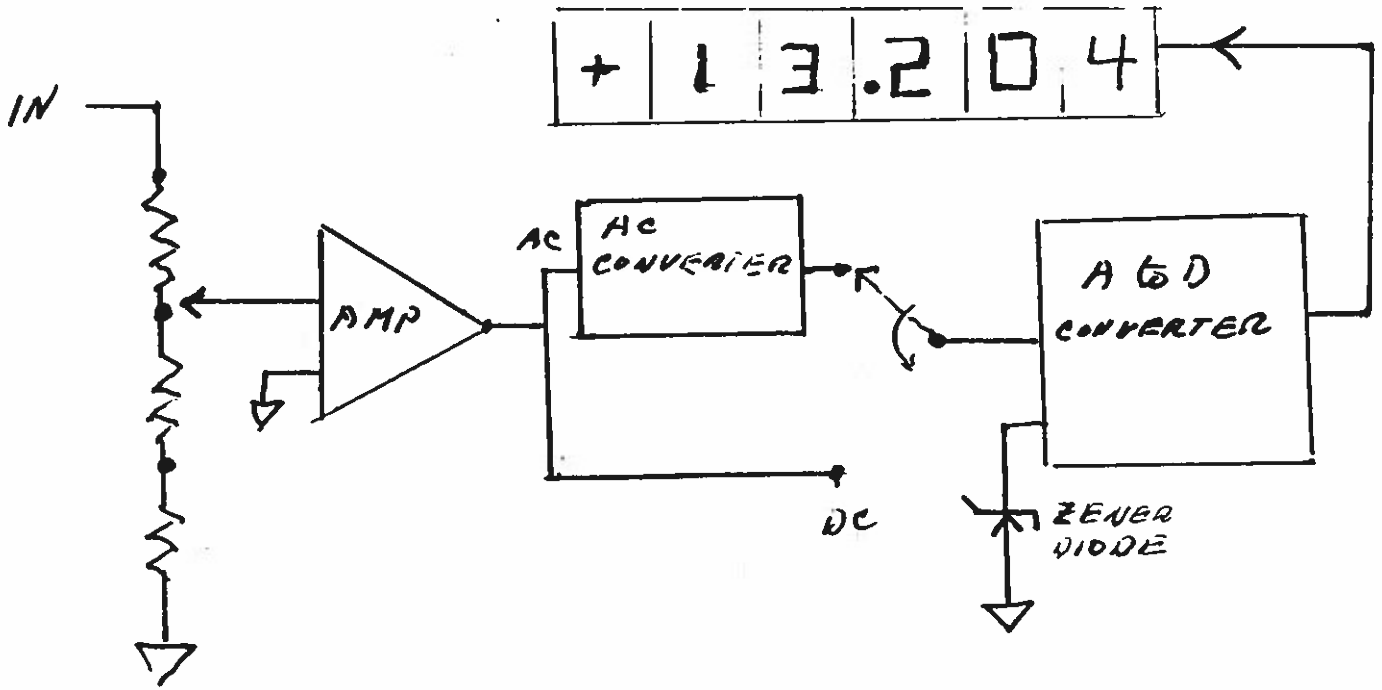
$$V_{RMS} = .707\, V_{PEAK}$$



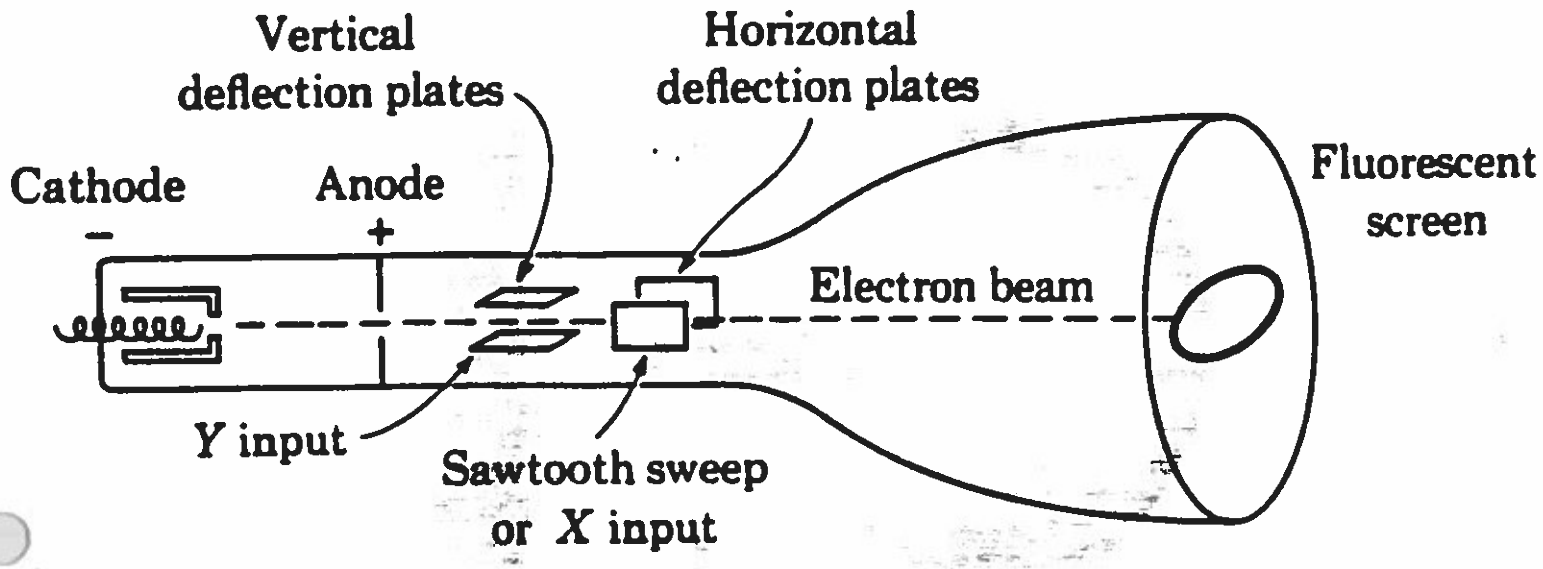
SIMPSON 260-7 VOLT-OHM-MILLIAMMETER



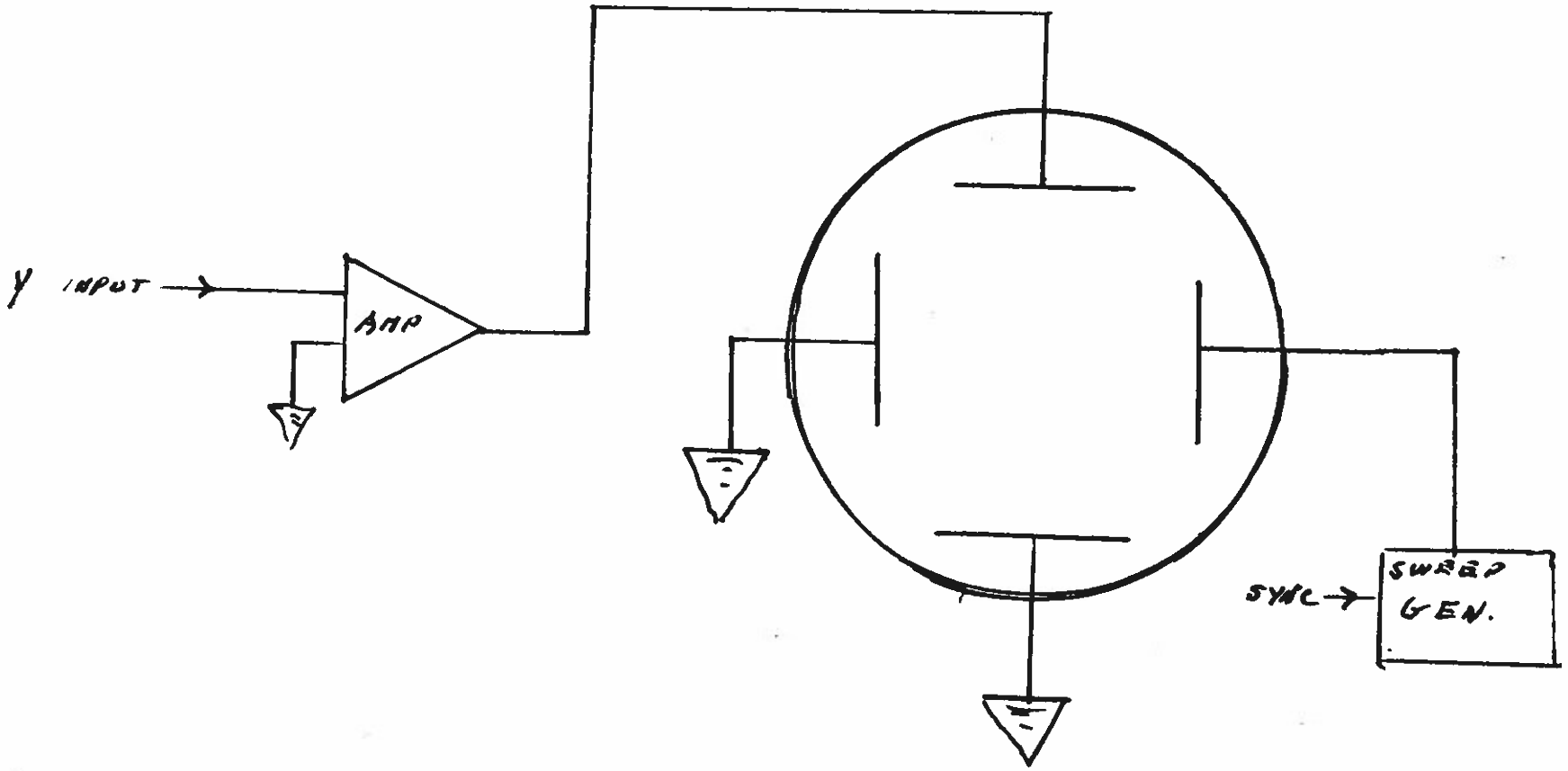
8050A Digital Multimeter



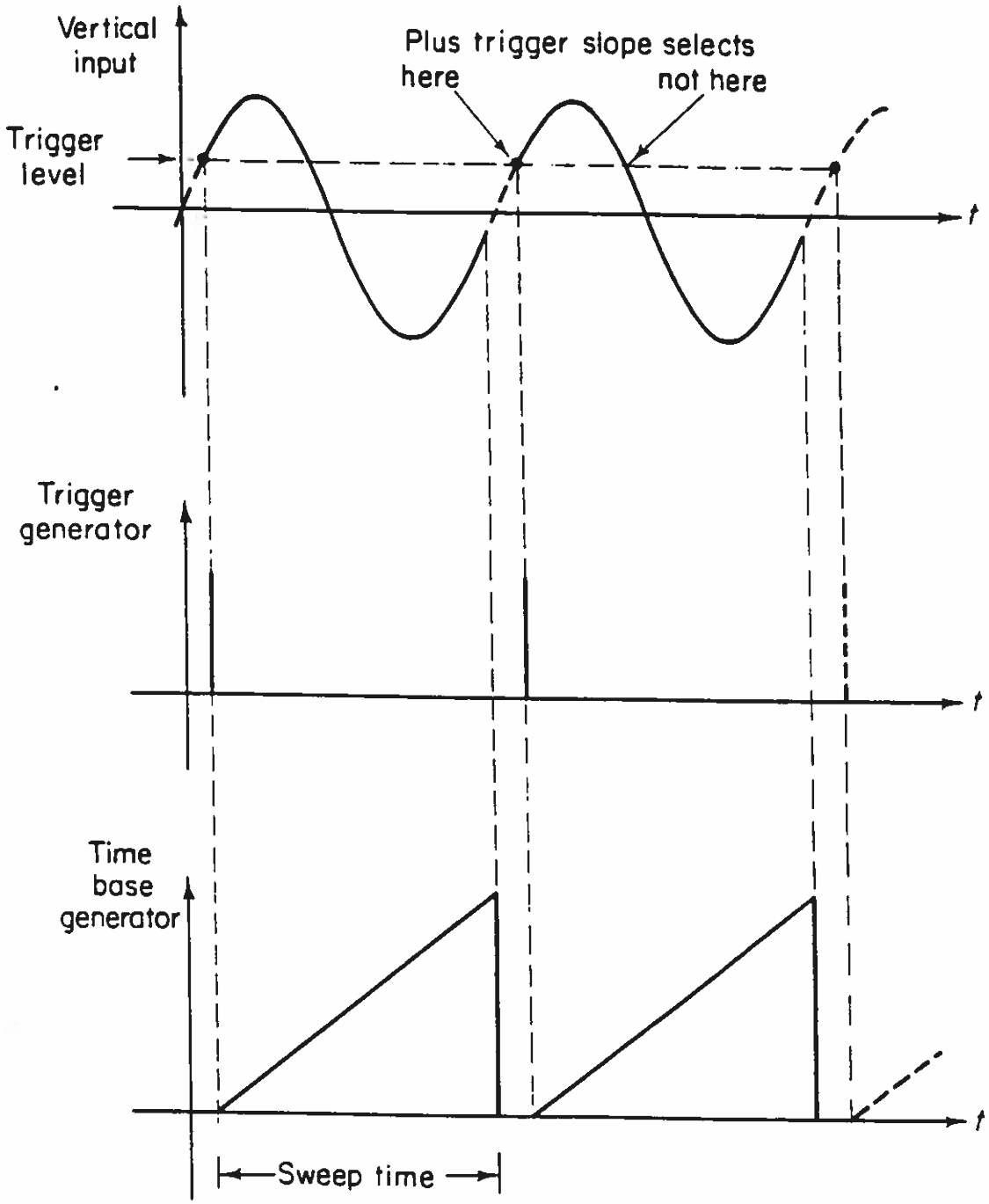
DIGITAL VOLTMETER

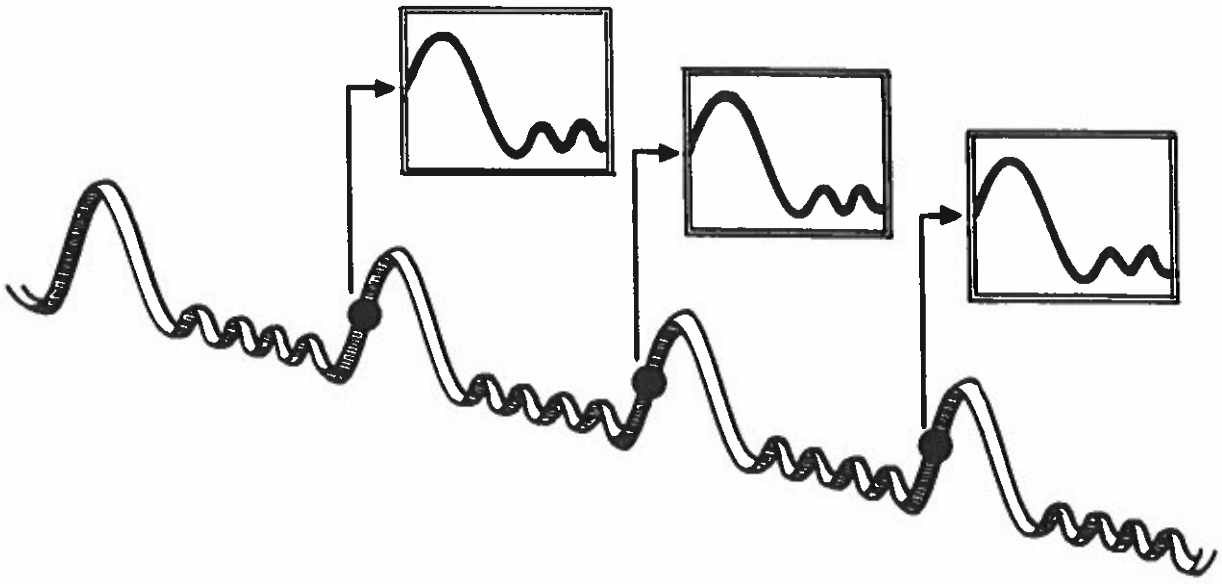


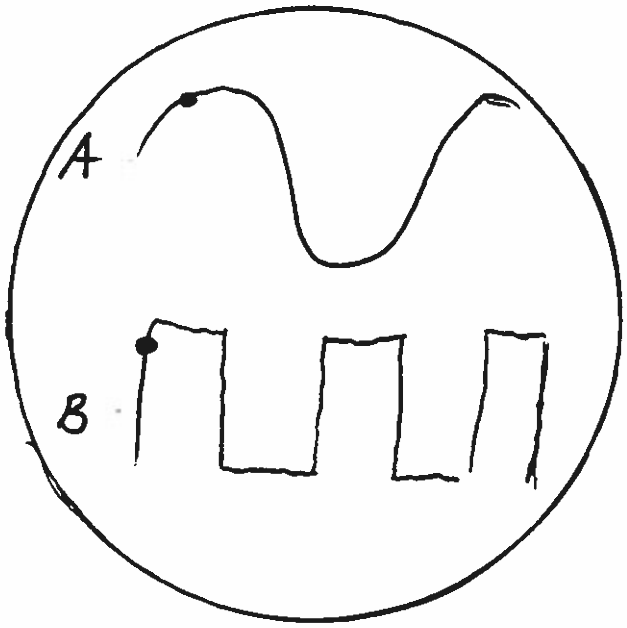
cathode-ray tube



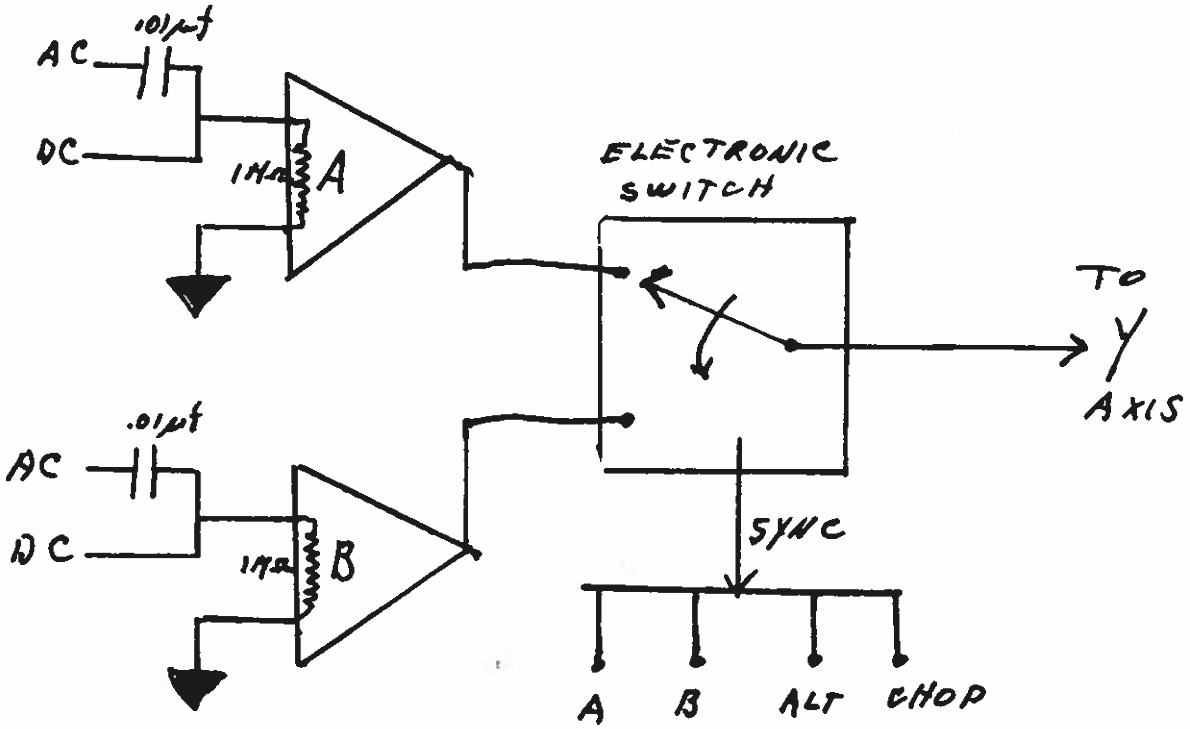
BASIC SCOPE


Vertical input
Plus trigger slope selects here
not here
Trigger level
t
Trigger generator
t
Time base generator
t
Sweep time





DUAL CHANNEL

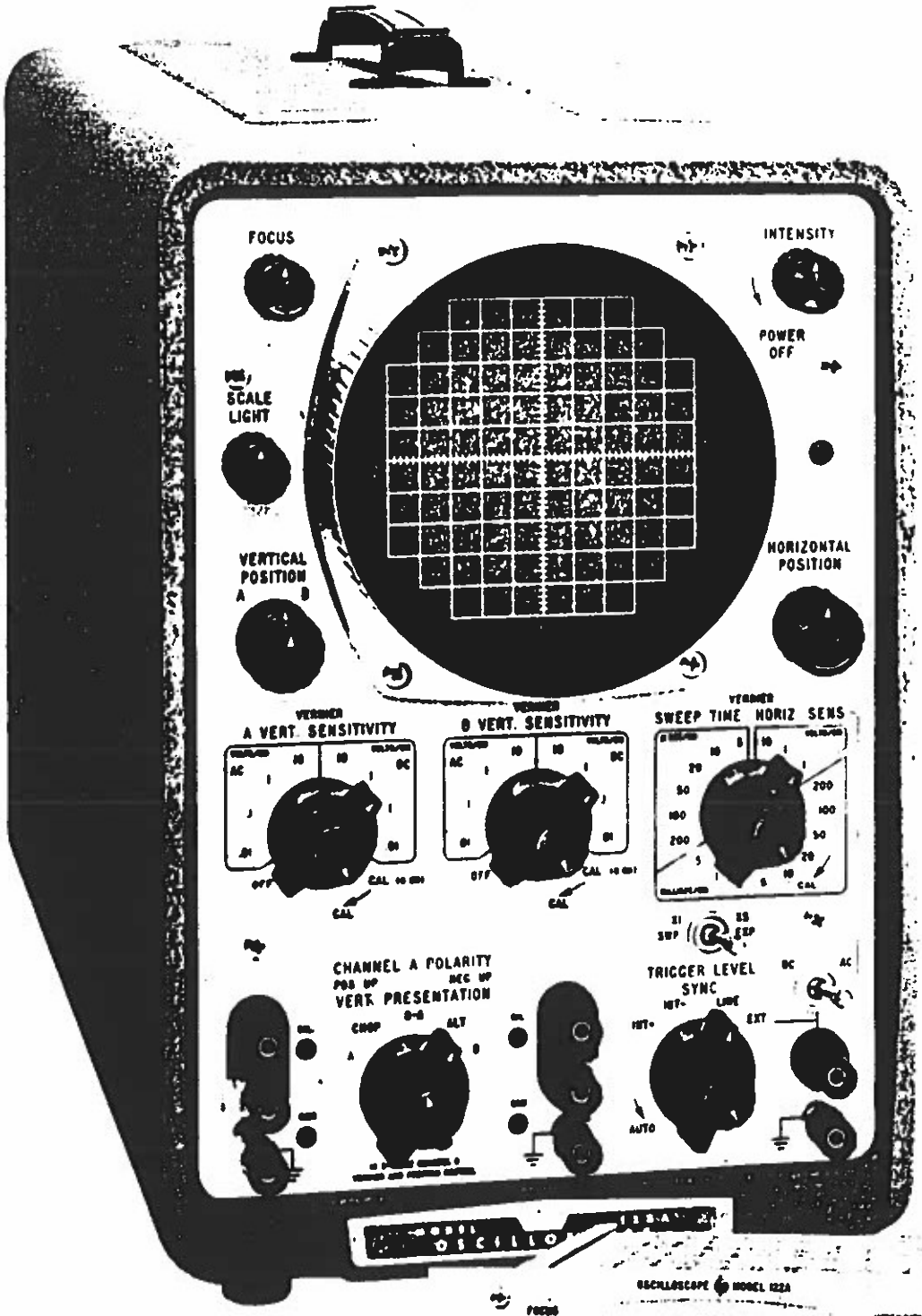


INPUT OPTIONS

MODEL 122A/AR

OSCILLOSCOPE

SERIALS PREFIXED: 006-



THE SPECTRUM ANALYZER —

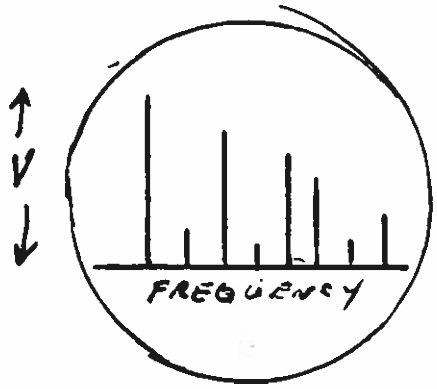
WHO NEEDS IT?

OSCILLOSCOPE PLOTS VOLTAGE vs TIME

SPECTRUM ANALYZER — VOLTAGE vs FREQ.

SCOPE → TIME DOMAINE

SPECTRUM ANALYZER → FREQ. DOMAINE



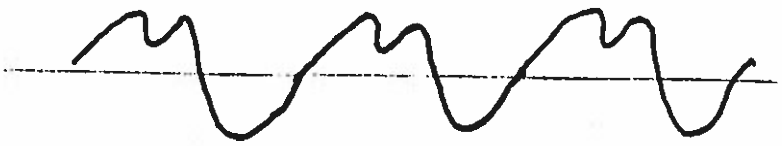
MATHAMETICALLY DEFINED WAVEFORMS

IMPULSE 

STEP 

RAMP 

SINE 

WHAT ABOUT: 

FOURIER THEOREM

ANY PERIODIC FUNCTION CAN BE EXPRESSED AS A CONSTANT TERM PLUS AN INFINITE SERIES OF SINES AND COSINES

$$f(t) = A + B_1 \sin \omega t + B_2 \sin 2\omega t \ldots + B_N \sin N\omega t + C_1 \cos \omega t + C_2 \cos 2\omega t \ldots + C_N \cos N\omega t$$

OR:

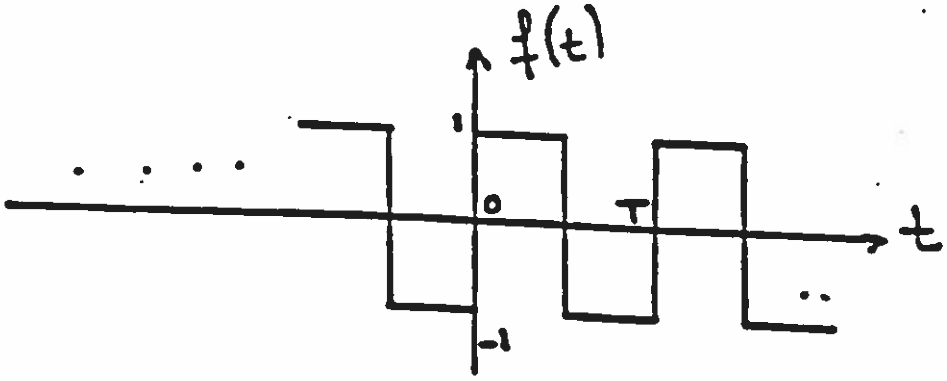
$$f(t) = A + D_1 \sin(\omega t + \phi_1) + D_2 \sin(2\omega t + \phi_2) + D_3 \sin(3\omega t + \phi_3) \ldots + D_N \sin(N\omega t + \phi_N)$$

WHERE $D = \sqrt{B^2 + C^2}$

AND $\phi = \tan^{-1} \frac{C}{B}$

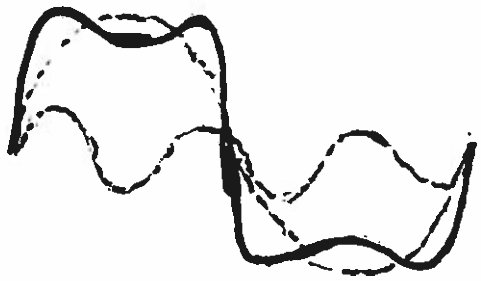
THE SPECTRUM ANALYZER GIVES US THE COEFFICIENTS OF ALL THE SINE TERMS.

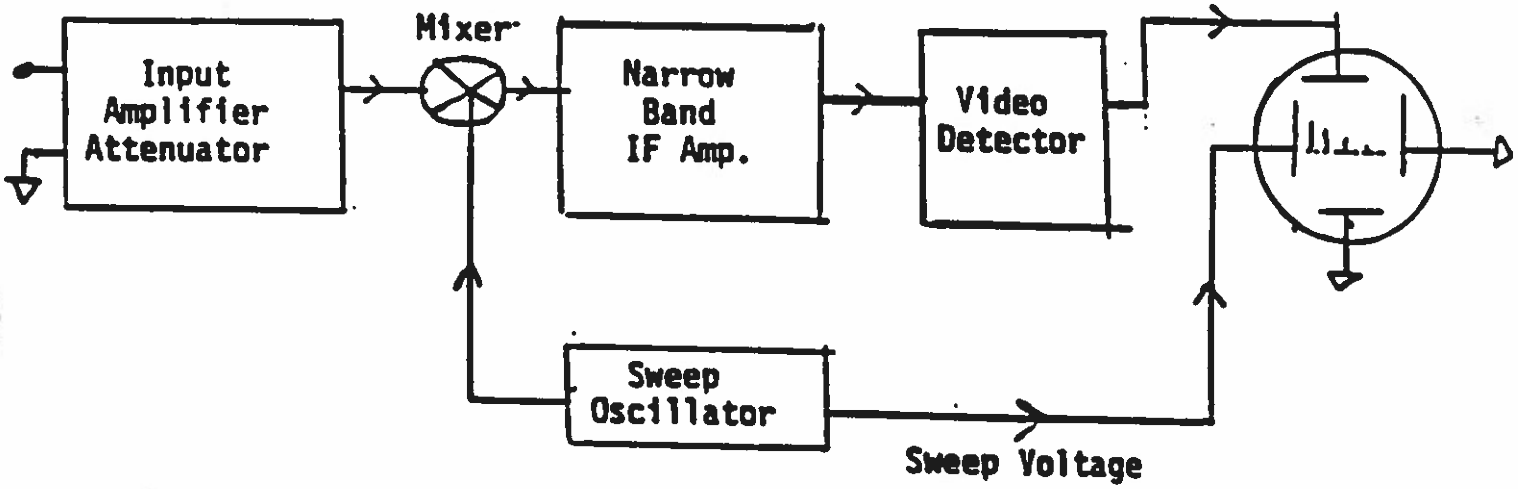
Square wave:



$$f(t) = \frac{4}{\pi}\left(\sin \omega_0 t + \frac{1}{3}\sin 3\omega_0 t + \frac{1}{5}\sin 5\omega t + \cdots\right)$$

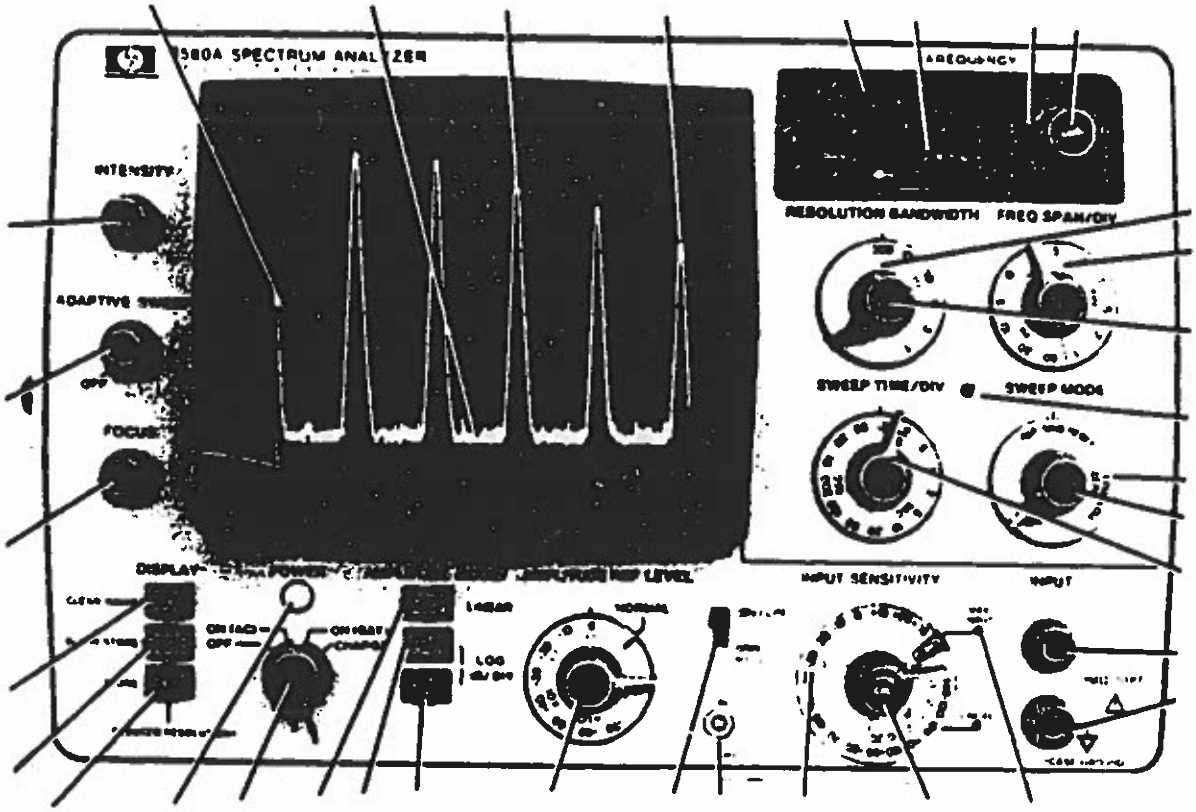
where $\omega_0 = \frac{2\pi}{T}$

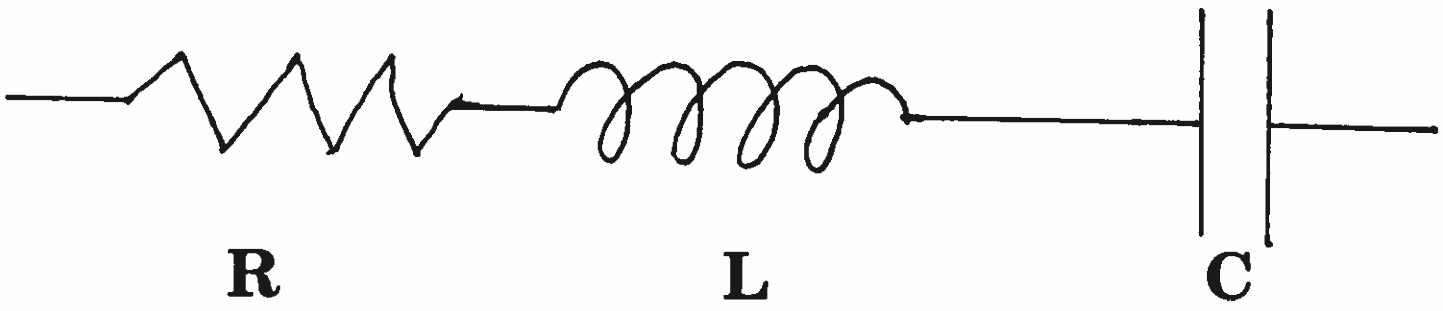




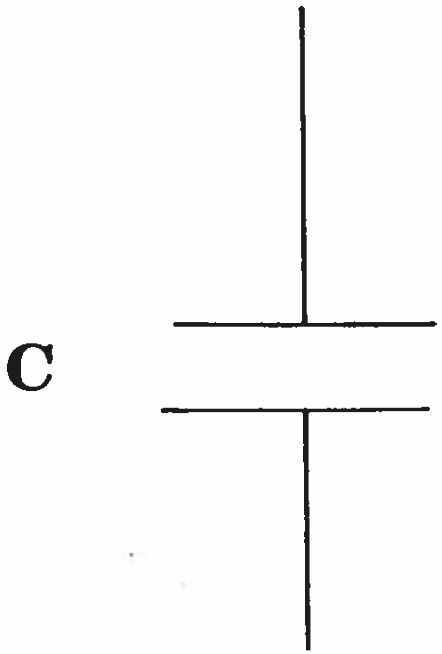
SPECTRUM ANALYZER

CB 1/10/90

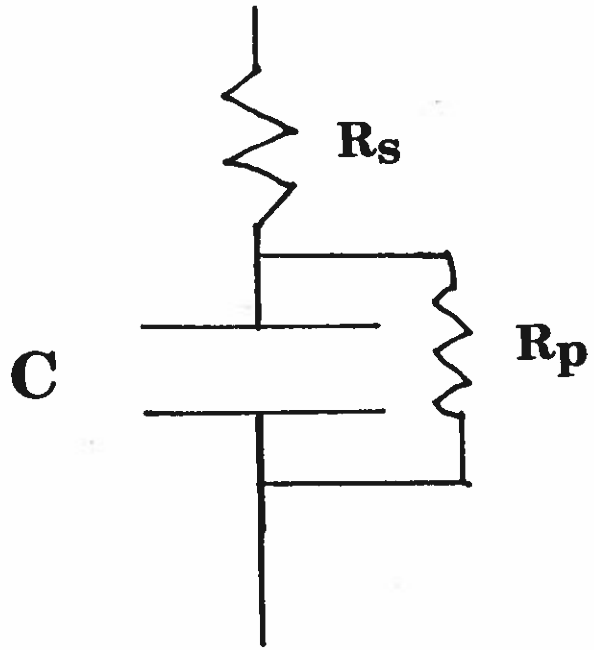

INTENSITY
FOCUS
FREQUENCY
RESOLUTION BANDWIDTH
FREQ SPAN/DIV
SWEEP TIME/DIV
SWEEP MODE
INPUT SENSITIVITY
INPUT
DISPLAY
LINEAR
LOG


R
L
C

Capacitors

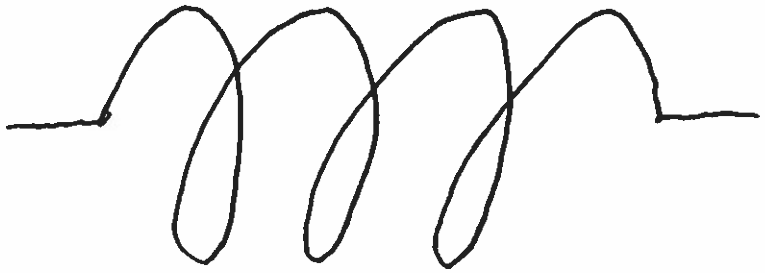


Ideal



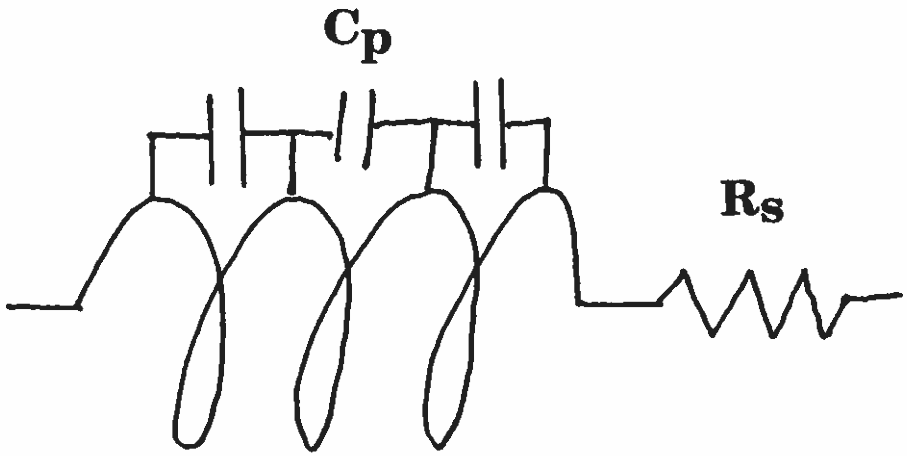
Actual

Inductors



L

Ideal



L

Actual

Quality Factor

$$Q = 2\pi \frac{\text{Peak energy stored per cycle}}{\text{Peak energy disipated per cycle}}$$

For inductors: $$Q = \frac{2\pi fL}{R}$$

For capacitors: $$Q = \frac{1}{2\pi fRC}$$

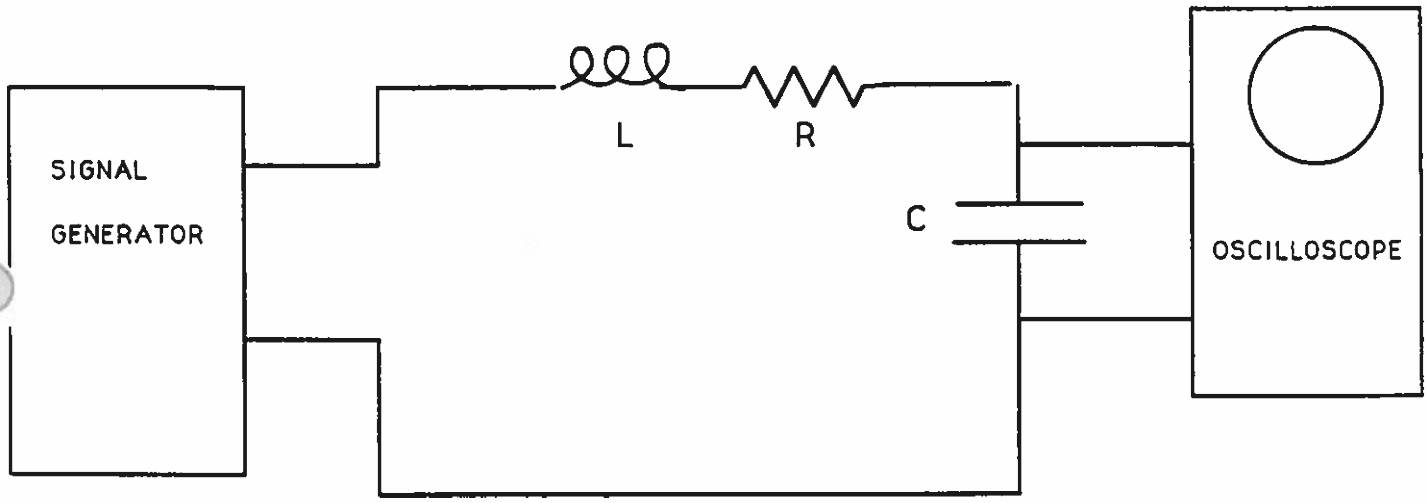
Note that **R** is series resistance for these formulae.

For practical components, loss for inductors is generally expressed as series resistance (copper loss). Loss for capacitors is typically expressed as a parallel resistance (leakage current across the capacitor).

Disipation Factor

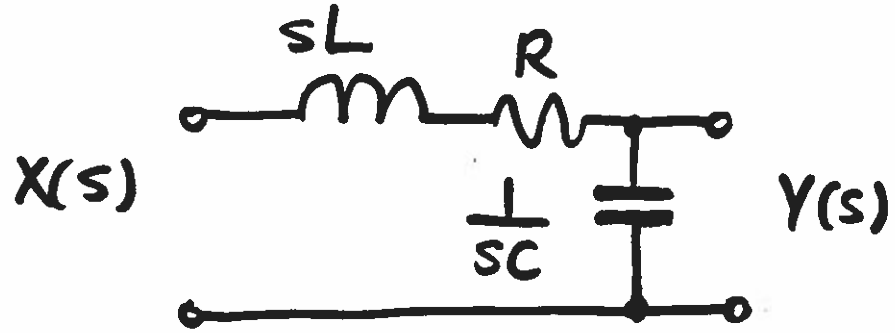
$$D = \frac{1}{Q}$$

Normally used to express loss in capacitors



R L C

Second Order System



- transfer function:

$$T(s) = \frac{Y(s)}{X(s)} = \frac{\frac{1}{sC}}{sL + R + \frac{1}{sC}}$$

$$= \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$$

define:

$$\begin{cases} \text{natural frequency:} & \omega_n \triangleq \frac{1}{\sqrt{LC}} \\ \text{damping ratio:} & \zeta \end{cases} \triangleq \frac{R}{2}\sqrt{\frac{C}{L}}$$

$$T(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

- Frequency Response: let $s = j\omega$

$$H(\omega) = T(j\omega) = \frac{\omega_n^2}{-\omega^2 + 2\zeta\omega_n j\omega + \omega_n^2}$$

$$= \frac{1}{1 - \left(\frac{\omega}{\omega_n}\right)^2 + j\,2\zeta\frac{\omega}{\omega_n}}$$

- Bode plot:

$$20\log_{10}|H(\omega)| = -10\log_{10}\left\{\left[1 - \frac{\omega^2}{\omega_n^2}\right]^2 + \left[2\zeta\frac{\omega}{\omega_n}\right]^2\right\}$$

$\omega \ll \omega_n$, $\omega/\omega_n \to 0$:

$$20\log_{10}|H(\omega)| \doteq -10\log_{10} 1 = 0$$

$\omega \gg \omega_n$

$$20\log_{10}|H(\omega)| \doteq -40\log_{10}\left(\frac{\omega}{\omega_n}\right)$$

$\omega = \omega_n$

$$20\log_{10}|H(\omega)| = -20\log_{10} 2\zeta \quad \left(\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}, \; R\sqrt{\frac{C}{L}}\right)$$

$$= 20\log_{10} Q$$

$$Q \triangleq \frac{1}{2\zeta}$$: sharpness of peak

$$\angle H(\omega) = -tg^{-1}\frac{2\zeta\frac{\omega}{\omega_n}}{1-\left(\frac{\omega}{\omega_n}\right)^2}$$

$\omega \ll \omega_n$

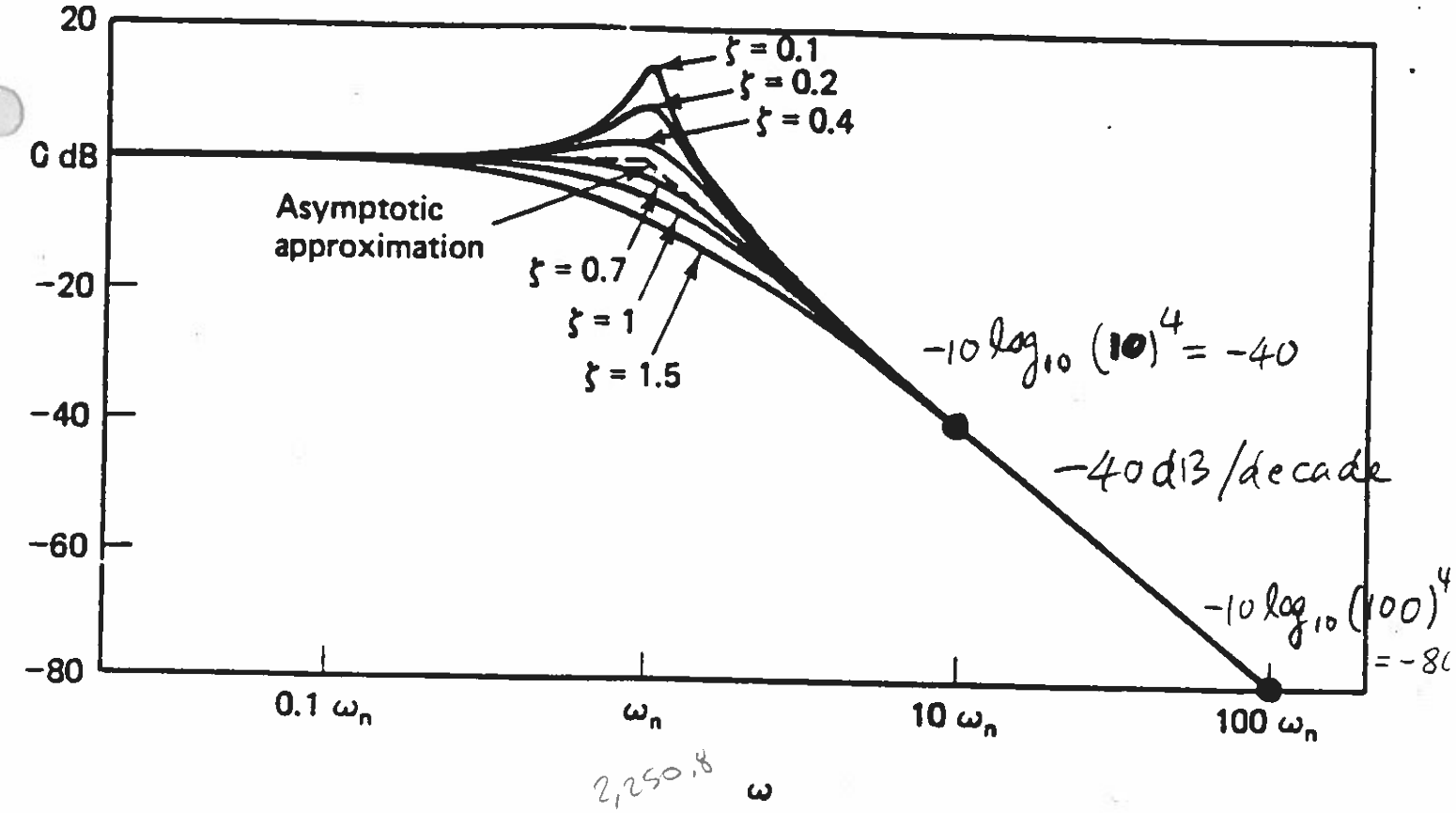
$$\angle H(\omega) \doteq -tg^{-1}(+0) = 0$$

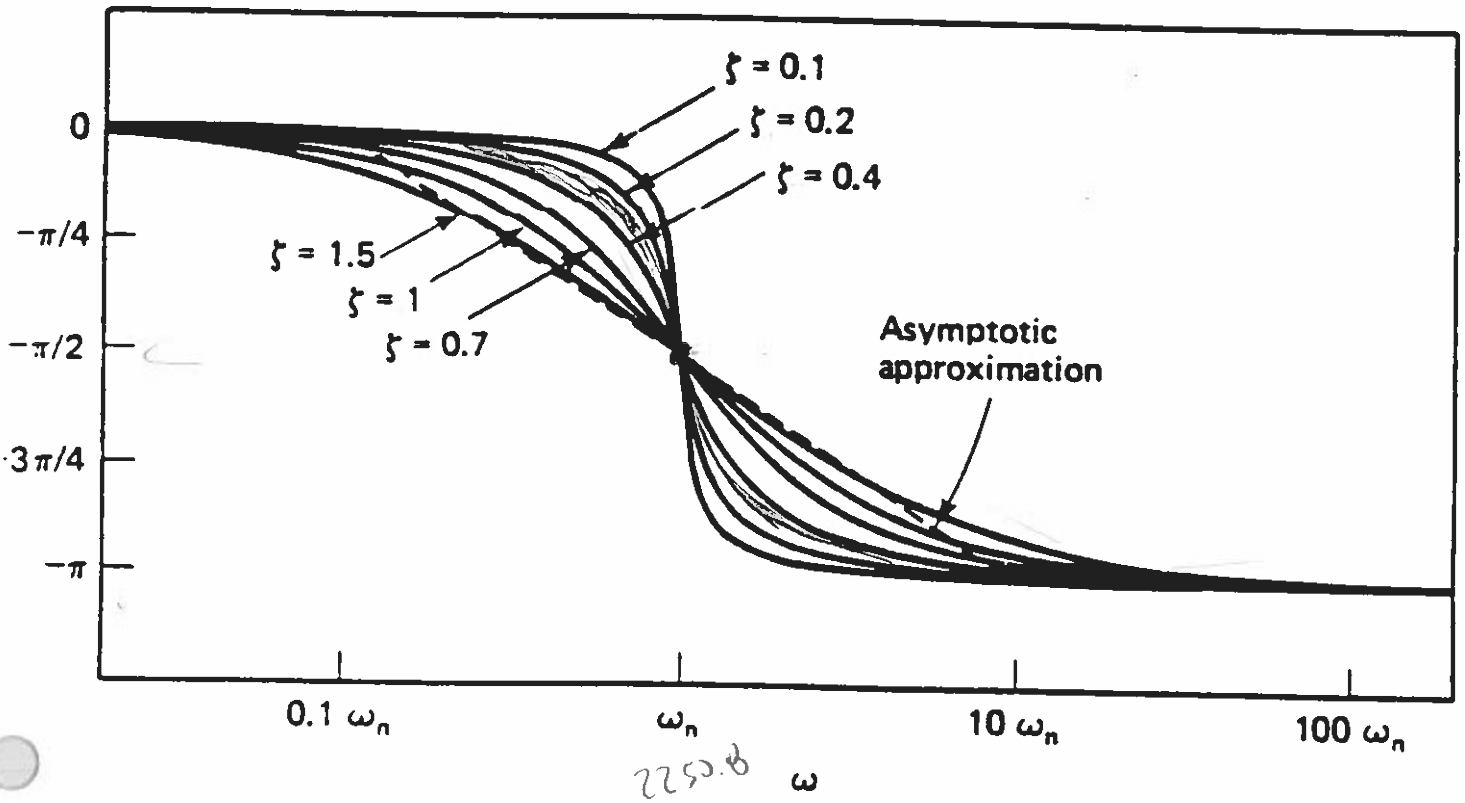
$\omega \gg \omega_n$

$$\angle H(\omega) \doteq -tg^{-1}(-0) = -\pi$$

$\omega = \omega_n$

$$\angle H(\omega) = -tg^{-1}(+\infty) = -\frac{\pi}{2}$$





Bode plots for second-order systems with several different values of damping ratio ζ.

- Find peak frequency ω_p: $|H(\omega_p)| = m$

$$H(\omega) = \frac{1}{1-\left(\frac{\omega}{\omega_n}\right)^2 + j2\zeta\frac{\omega}{\omega_n}}$$

$$|H(\omega)| = \frac{1}{\left\{\left[\left(\frac{\omega}{\omega_n}\right)^2-1\right]^2 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2\right\}^{1/2}}$$

want to find $\omega = \omega_p$, so that $|H(\omega_p)|$ is the maximum.

Consider

$$G(\omega) = \frac{1}{|H(\omega)|^2} = \left[\left(\frac{\omega}{\omega_n}\right)^2-1\right]^2 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2$$

let $u = \left(\frac{\omega}{\omega_n}\right)^2$

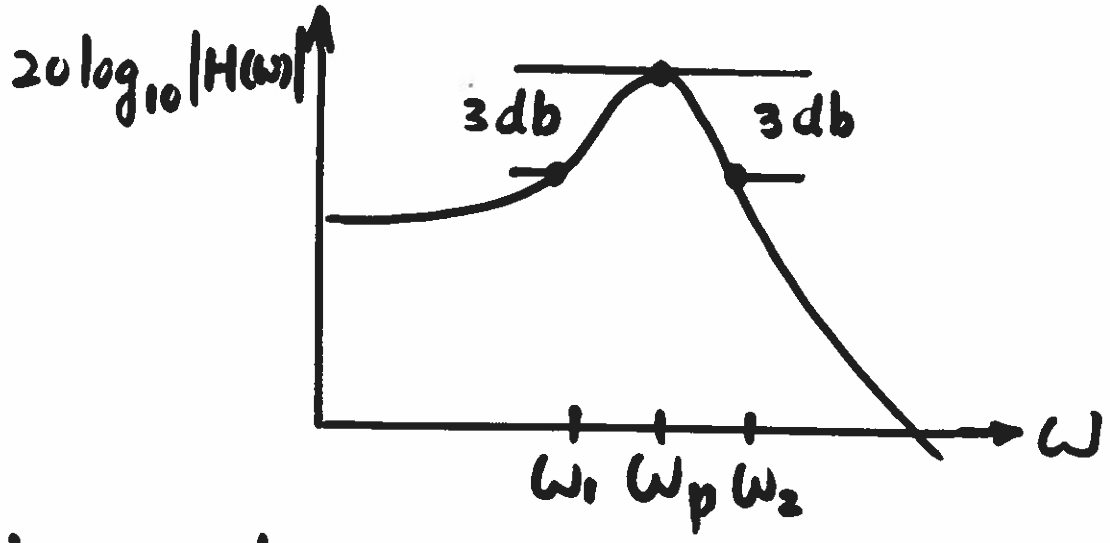
$$G(u) = (u-1)^2 + 4\zeta^2 u = u^2 + (4\zeta^2-2)u + 1$$

$$\frac{d}{du}G(u) = 2u + 4\zeta^2 - 2 = 0 \rightarrow u_p = 1-2\zeta^2$$

$$\left(\frac{\omega_p}{\omega_n}\right)^2 = 1-2\zeta^2, \quad \omega_p = \omega_n\sqrt{1-2\zeta^2}$$

$$|H(\omega_p)| = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \doteq \frac{1}{2\zeta}$$

- Find bandwidth $\Delta\omega = \omega_2 - \omega_1$



$$\frac{|H(\omega_p)|}{|H(\omega_1)|} = \sqrt{2} = \frac{1}{0.707}$$

again, let $u = \left(\frac{\omega}{\omega_n}\right)^2$

$$|H(\omega_1)| = \frac{1}{\sqrt{(u-1)^2 + 4\zeta^2 u}}$$

and $$|H(\omega_p)| \doteq \frac{1}{2\zeta\sqrt{1-\zeta^2}}$$

$$\therefore \frac{|H(\omega_p)|}{|H(\omega_1)|} = \frac{\sqrt{(u-1)^2 + 4\zeta^2 u}}{2\zeta\sqrt{1-\zeta^2}} = \sqrt{2}$$

$$u^2 + (4\zeta^2 - 2)u + 1 - 8\zeta^2(1-\zeta^2) = 0$$

$$u_1, u_2 = (1 - 2\zeta^2) \pm 2\zeta\sqrt{1-\zeta^2}$$

$$\begin{cases} \omega_1 = \sqrt{u_1}\,\omega_n \\ \omega_2 = \sqrt{u_2}\,\omega_n \end{cases}$$

$$\Delta\omega = \omega_2 - \omega_1 = (\sqrt{u_2} - \sqrt{u_1})\,\omega_n$$

Further, consider

$$u_2 - u_1 = (\sqrt{u_2} + \sqrt{u_1})(\sqrt{u_2} - \sqrt{u_1})$$

$$= 4\zeta\sqrt{1-\zeta^2}$$

assume $\sqrt{u_p} \doteq \frac{1}{2}(\sqrt{u_2} + \sqrt{u_1})$

then $\sqrt{u_2} - \sqrt{u_1} = \frac{1}{2\sqrt{u_p}}\, 4\zeta\sqrt{1-\zeta^2}$

$$= \frac{2\zeta\sqrt{1-\zeta^2}}{\sqrt{1-2\zeta^2}} \doteq 2\zeta$$

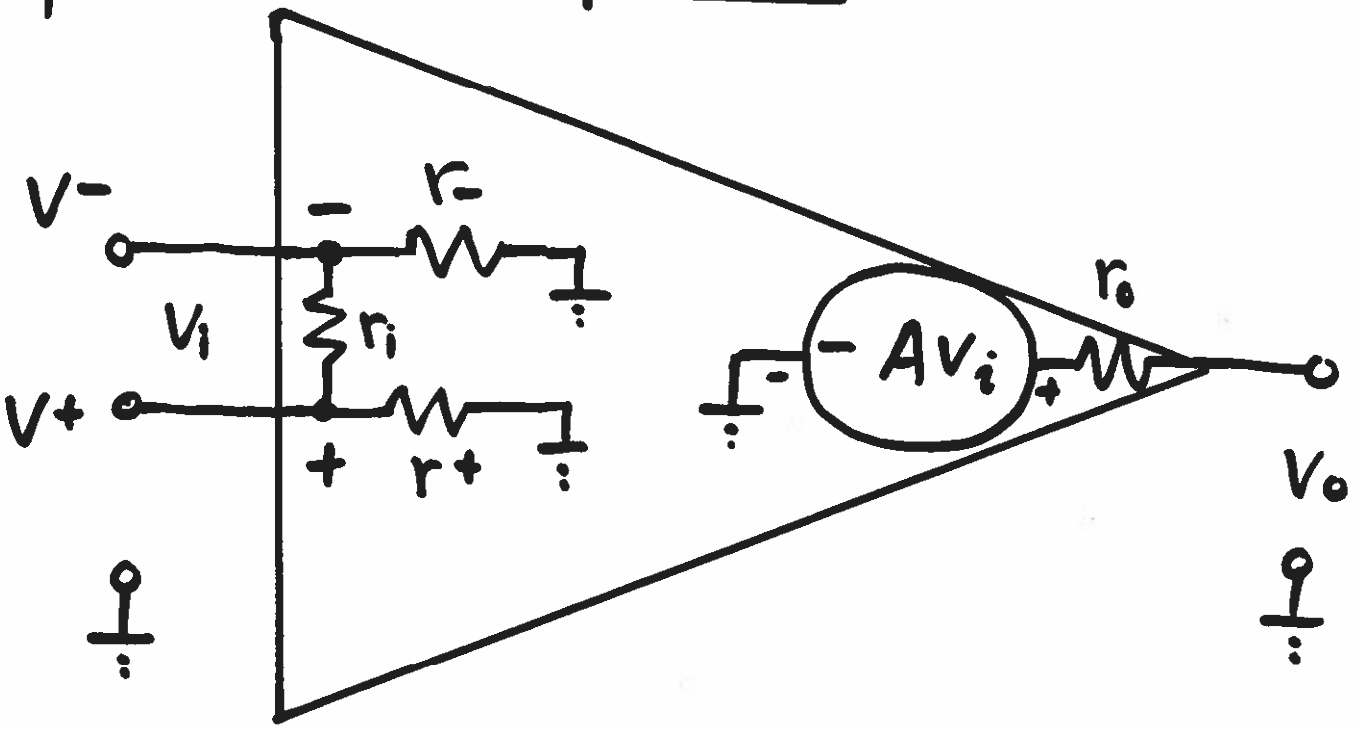
$\therefore\ \Delta\omega = \omega_n(\sqrt{u_2} - \sqrt{u_1}) \doteq 2\zeta\omega_n$

$$\begin{cases} \text{Peak frequency: } \omega_p = \omega_n \sqrt{1-2\zeta^2} \\ \text{Bandwidth: } \Delta\omega \doteq 2\zeta\omega_n \end{cases}$$

re write transfer function:

$$T(s) = \frac{\omega_n^2}{s^2 + \Delta\omega\, s + \omega_n^2}$$

Operational Amplifier



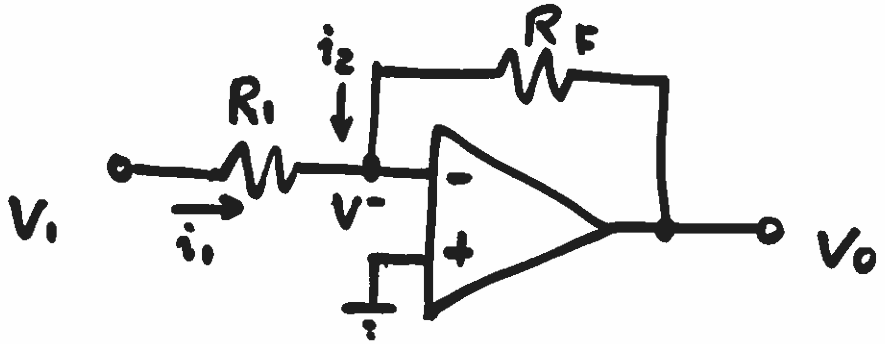
assumptions:

$A \to \infty$, $v_i = V^+ - V^- \to 0$ $(V^+ \doteq V^-)$

(V_o still finite)

$r_i, r_-, r_+ \to \infty$, $r_o \to 0$

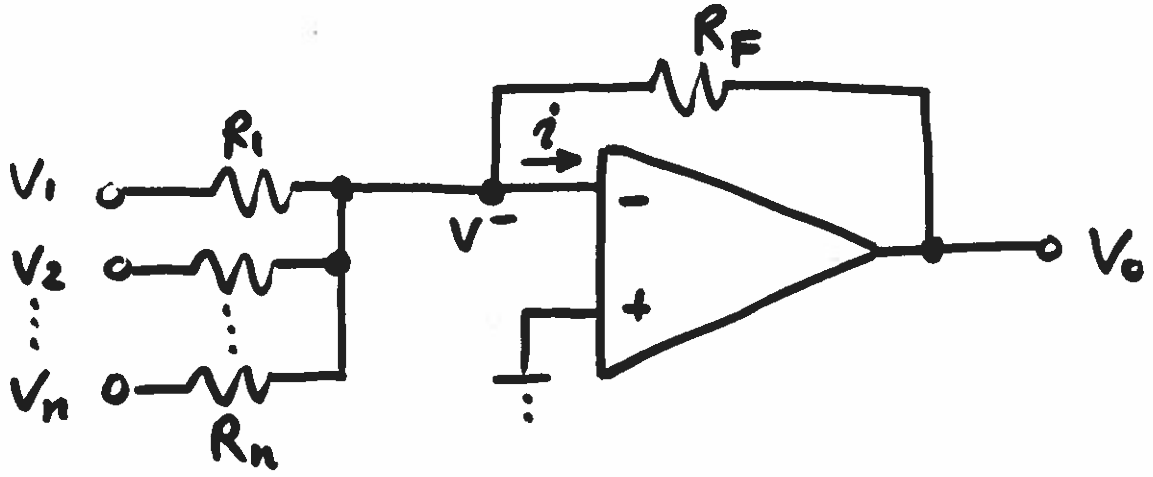
- Inverter



$$i_1 + i_2 = \frac{V^- - V_1}{R_1} + \frac{V^- - V_o}{R_F} = 0 \quad , V^- \doteq 0$$

$$\therefore \quad \frac{V_o}{V_1} = -\frac{R_F}{R_1} \qquad \text{if } R_F = R_1 \quad V_o = -V_1$$

- Summer - inverter

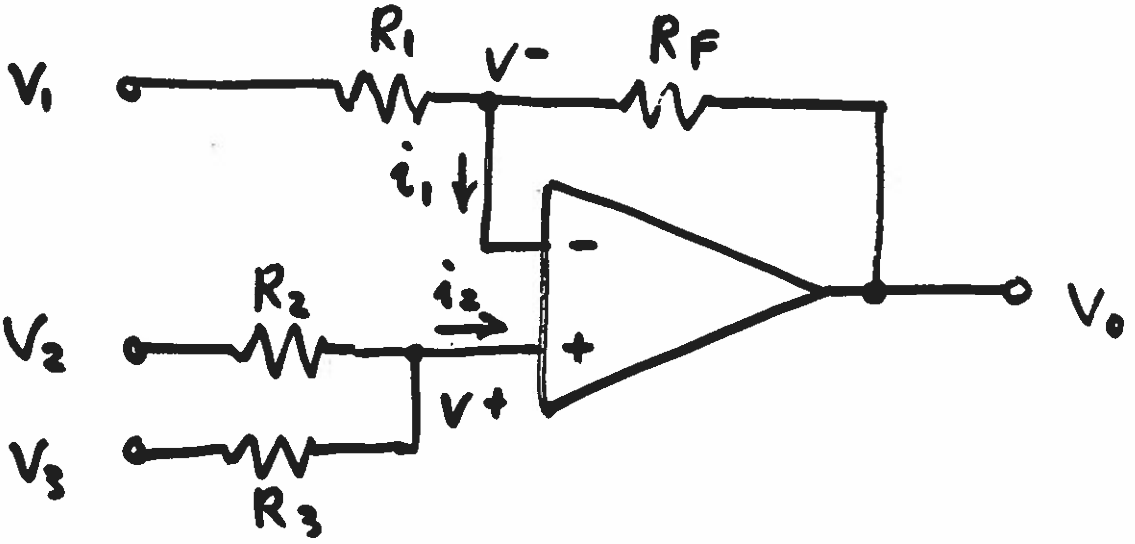


$$i = \sum_{j=1}^{n} \frac{V^- - V_j}{R_j} + \frac{V^- - V_o}{R_F} \doteq 0 \ , \ V^- \doteq 0$$

$$\therefore \ V_o = - R_F \sum_{j=1}^{n} \frac{V_j}{R_j} = - \sum_{j=1}^{n} k_j V_j$$

$$k_j = \frac{R_F}{R_j} \quad (j = 1, 2, \cdots n)$$

EX



$$V^- \doteq V^+ = V, \qquad i_1 = i_2 \doteq 0$$

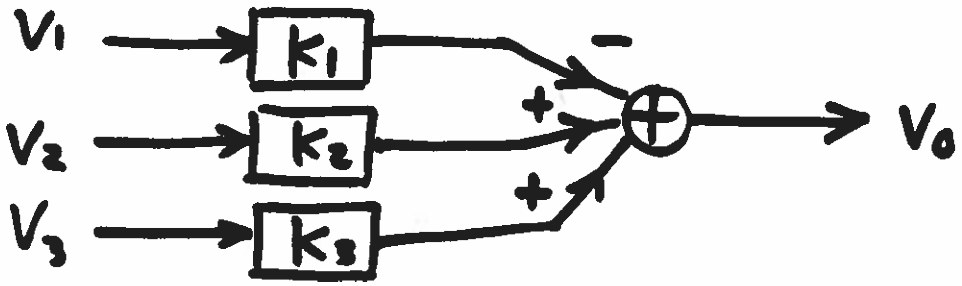
$$\begin{cases} \dfrac{V-V_1}{R_1} + \dfrac{V-V_0}{R_F} = 0 & (a) \\ \dfrac{V-V_2}{R_2} + \dfrac{V-V_3}{R_3} = 0 & (b) \end{cases}$$

from (b) $\quad V = \dfrac{R_2}{R_2+R_3}V_3 + \dfrac{R_3}{R_2+R_3}V_2$

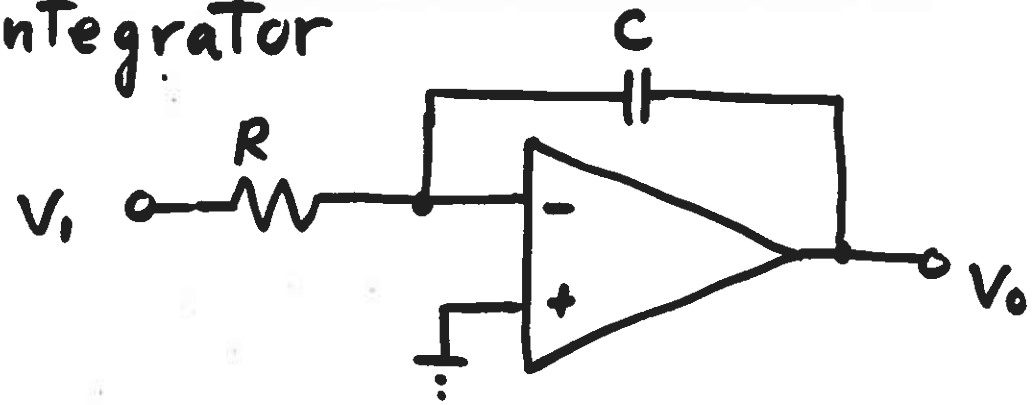
substitute in (a)

$$V_0 = \left(\frac{R_F}{R_1}+1\right)\left[\frac{R_2}{R_2+R_3}V_3 + \frac{R_3}{R_2+R_3}V_2\right] - \frac{R_F}{R_1}V_1$$

$$= -K_1V_1 + K_2V_2 + K_3V_3$$



- Integrator



Similar to inverter, we have

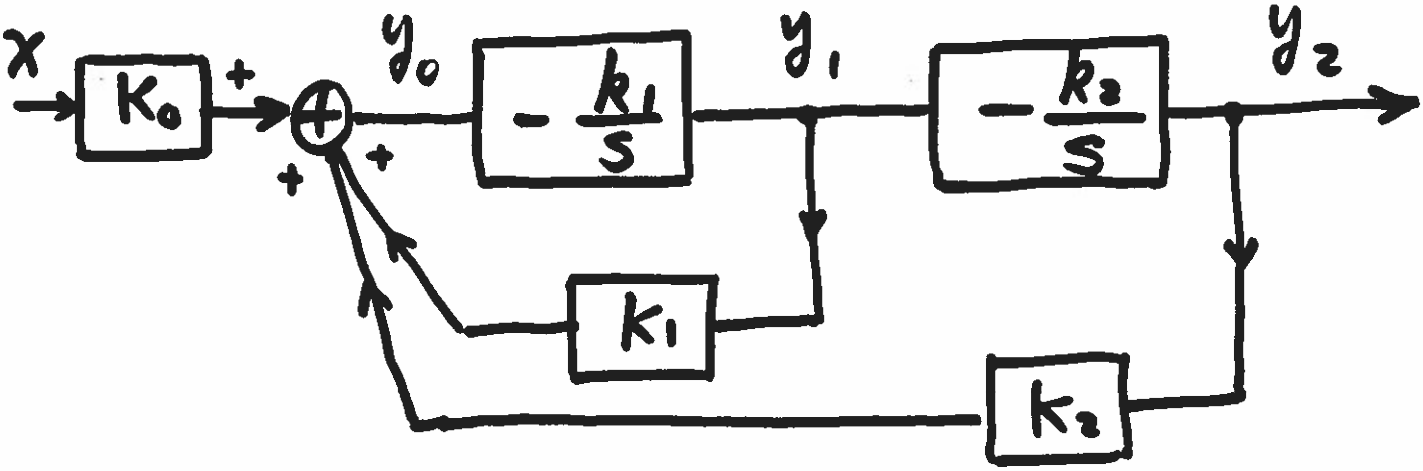
$$T(s)=\frac{V_o(s)}{V_i(s)}=-\frac{\frac{1}{sC}}{R}=-\frac{1}{RC\,s}$$

let $\frac{1}{RC}=k$

$$T(s)=-\frac{k}{s}$$

First order system

Construct 2nd Order System with Integrators



$$y_1 = -\frac{k_1}{s} y_0 \quad , \quad y_2 = -\frac{k_2}{s} y_1$$

$$y_1 = -\frac{s}{k_2} y_2 \quad . \quad y_0 = \frac{s^2}{k_1 k_2} y_2$$

$$y_0 = K_0 x + k_1 y_1 + k_2 y_2$$

$$\frac{s^2}{k_1 k_2} y_2 = K_0 x + k_1 \left(-\frac{s}{k_2}\right) y_2 + k_2 y_2$$

$$T(s) = \frac{y_2}{x} = \frac{K_0}{\frac{s^2}{k_1 k_2} - \frac{s}{k_2} s - k_2}$$

$$= \frac{k_1 k_2 K_0}{s^2 + k_1 k_1 s - k_1 k_2 k_2}$$

if $k_1 = k_2 = k$

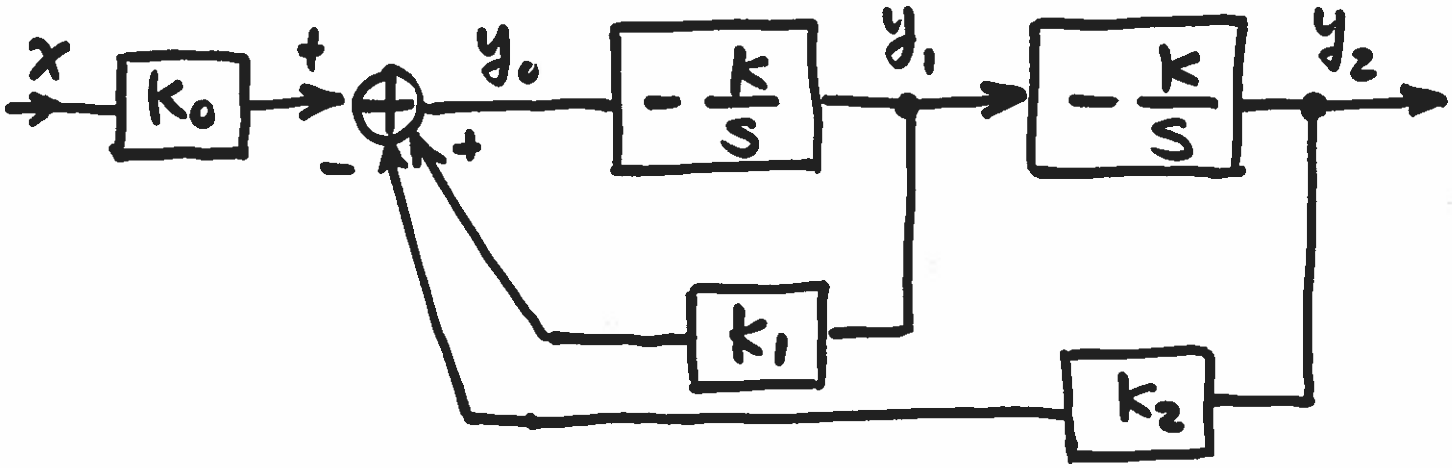
$$T(s) = \frac{k^2 K_0}{s^2 + k_1 k s - k_2 k^2}$$

Compare with

$$T(s) = \frac{\omega_n^2}{s^2 + \Delta\omega s + \omega_n^2}$$

We see that $k_2 < 0$

i.e.



E-54
Digital logic

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

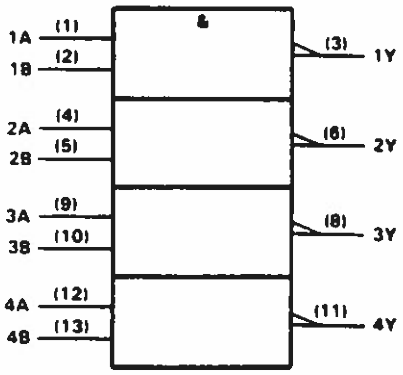
These devices contain four independent 2-input-NAND gates.

The SN5400, SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

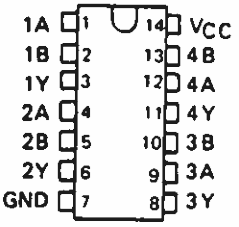
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol†

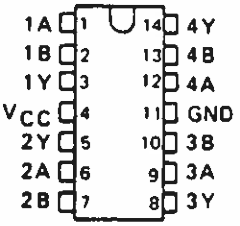


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

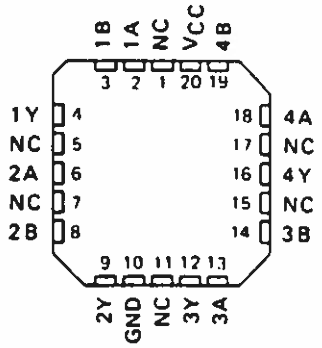
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400 . . . N PACKAGE
SN74LS00, SN74S00 . . . D OR N PACKAGE
(TOP VIEW)



SN5400 . . . W PACKAGE
(TOP VIEW)

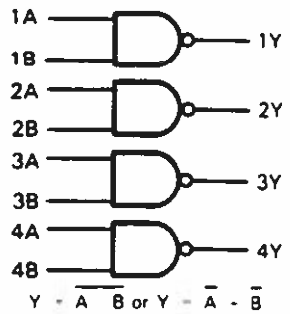


SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

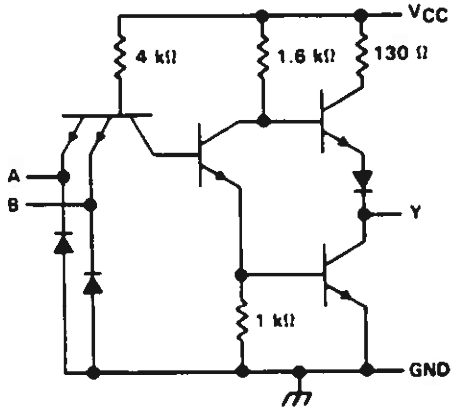
logic diagram (positive logic)



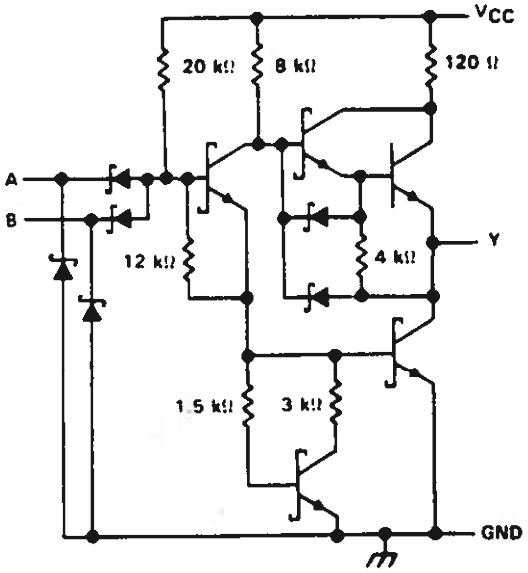
$Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

schematics (each gate)

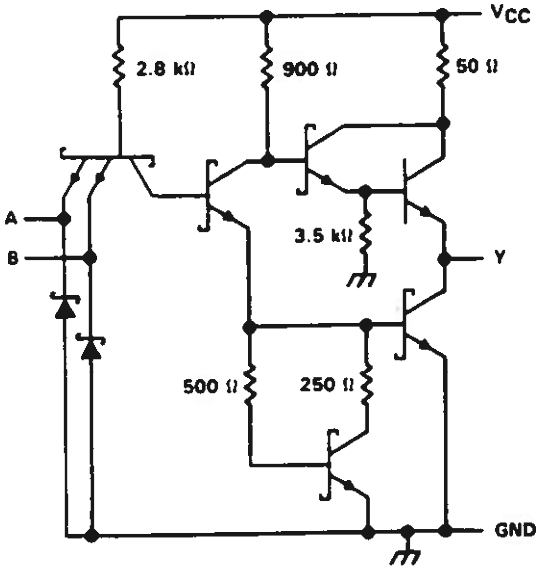
'00



'LS00



'S00



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '00, 'S00 . . . . . 5.5 V
'LS00 . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended c

V_{CC}	Supply volt
V_{IH}	High-level
V_{IL}	Low-level
I_{OH}	High-level
I_{OL}	Low-level
T_A	Operating

electrical chara

PARAMETER	
V_{IK}	
V_{OH}	
V_{OL}	
I_I	
I_{IH}	
I_{IL}	
I_{OS}§	
I_{CCH}	
I_{CCL}	

† For conditions s
‡ All typical value
§ Not more than c

switching char

PARAMETER	
t_{PLH}	
t_{PHL}	

NOTE 2: Load c

recommended operating conditions

		SN5400			SN7400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5400			SN7400			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		12	22		12	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11	22	ns
t_{PHL}					7	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

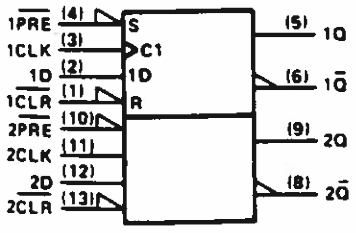
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

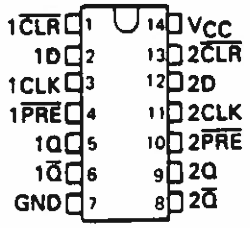
logic symbol‡



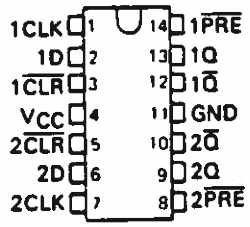
‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

§ Pin numbers shown are for D, J, N, and W packages.

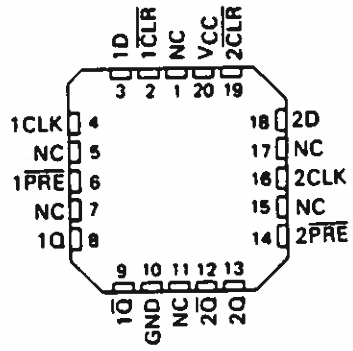
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

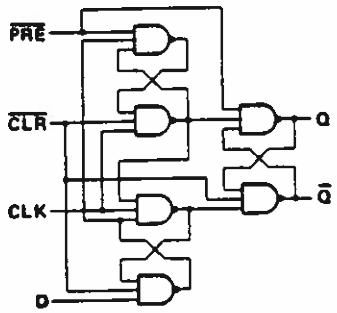


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



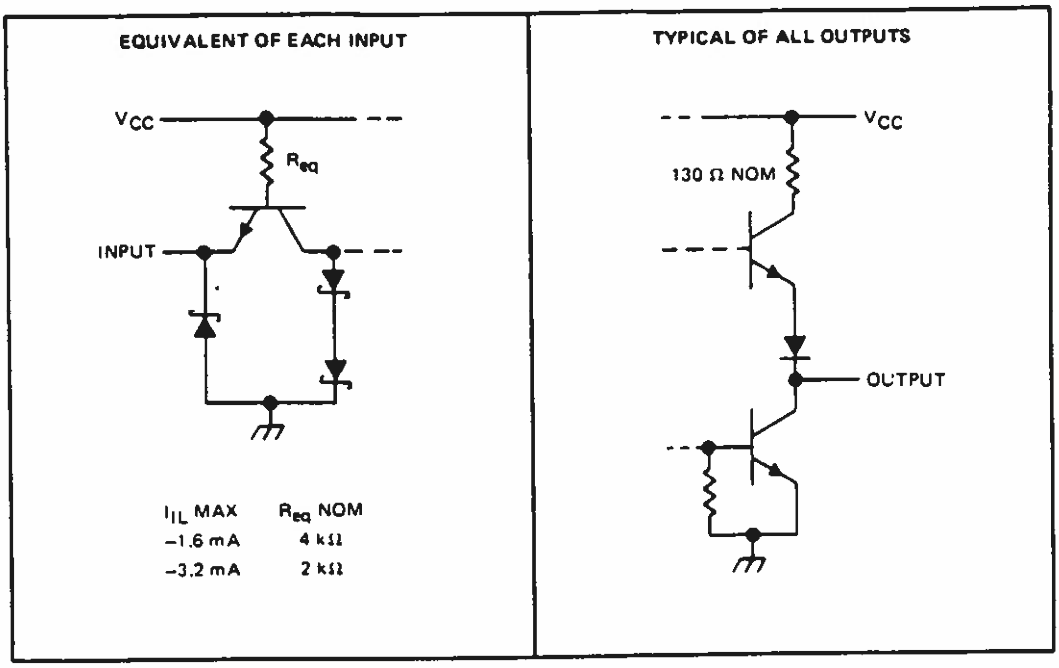
NC – No internal connection

logic diagram (positive logic)

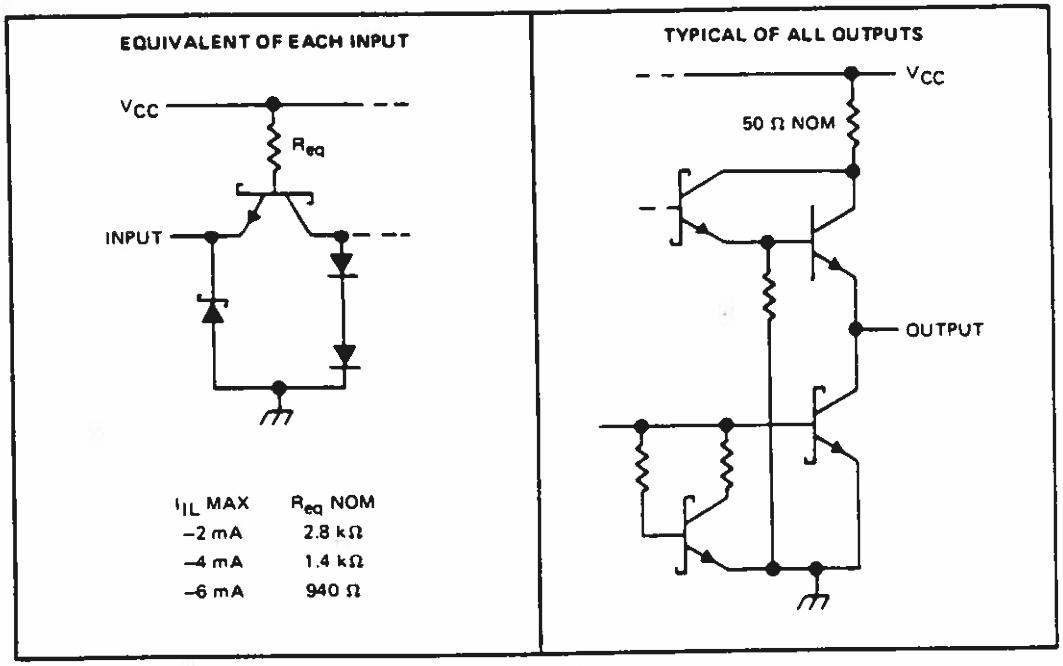


schematics of inputs and outputs

'74



'S74



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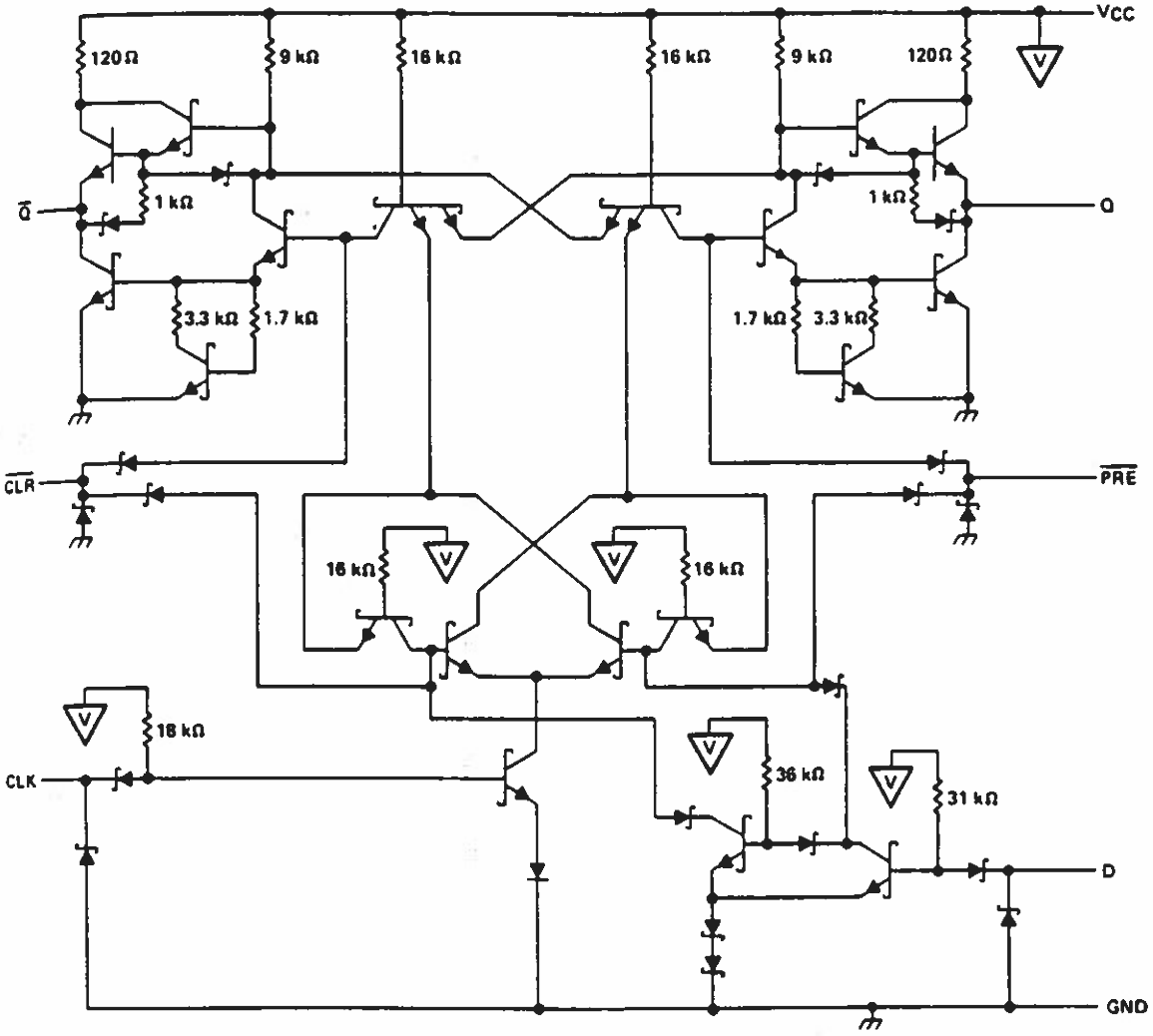
schematic

'LS74A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '74, 'S74 . . . . . 5.5 V
'LS74A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN5474			SN7474			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	30			30			ns
		CLK low	37			37			
		$\overline{PRE}$ or $\overline{CLR}$ low	30			30			
t_{su}	Input setup time before CLK↑		20			20			ns
t_h	Input hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN5474			SN7474			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	D	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
	$\overline{CLR}$						120			120	
	All Other						80			80	
I_{IL}	D	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
	$\overline{PRE}$§						−1.6			−1.6	
	$\overline{CLR}$§						−3.2			−3.2	
	CLK						−3.2			−3.2	
I_{OS}¶		V_{CC} = MAX			−20		−57	−18		−57	mA
I_{CC}#		V_{CC} = MAX,	See Note 2			8.5	15		8.5	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Clear is tested with preset high and preset is tested with clear high.
¶Not more than one output should be shown at a time.
#Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching charateristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	25		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$				25	ns
t_{PHL}						40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			14	25	ns
t_{PHL}					20	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

			SN54LS74A			SN74LS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time-before CLK↑	High-level data	20			20			ns
		Low-level data	20			20			
t_h	Hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS74A			SN74LS74A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = MAX,	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
I_I	D or CLK	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$						0.2			0.2	
I_{IH}	D or CLK	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	$\overline{CLR}$ or $\overline{PRE}$						40			40	
I_{IL}	D or CLK	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	$\overline{CLR}$ or $\overline{PRE}$						−0.8			−0.8	
I_{OS}		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX,	See Note 2			4	8		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$			13	25	ns
t_{PHL}					25	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			SN54S74			SN74S74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−1	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	6			6			ns
		CLK low	7.3			7.3			
		$\overline{CLR}$ or $\overline{PRE}$ low	7			7			
t_{su}	Setup time, before CLK ↑	High-level data	3			3			ns
		Low-level data	3			3			
t_h	Input hold time - data after CLK ↑		2			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S74			SN74S74			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA,			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	D	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
	$\overline{CLR}$				150			150	
	$\overline{PRE}$ or CLK				100			100	
I_{IL}	D	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
	$\overline{CLR}$¶				−6			−6	
	$\overline{PRE}$¶				−4			−4	
	CLK				−4			−4	
I_{OS}§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}#		V_{CC} = MAX, See Note 2		15	25		15	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶Clear is tested with preset high and preset is tested with clear high.
#Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 280 Ω, C_L = 15 pF	75	110		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			4	6	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q			9	13.5	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)				5	8	
t_{PLH}	CLK	Q or $\overline{Q}$			6	9	ns
t_{PHL}					6	9	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

DECEMBER 1972 – REVISED MARCH 1988

- **Designed Specifically for High-Speed:**
  Memory Decoders
  Data Transmission Systems
- **Two Fully Independent 2- to 4-Line Decoders/Demultiplexers**
- **Schottky Clamped for High Performance**

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The circuit comprises two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

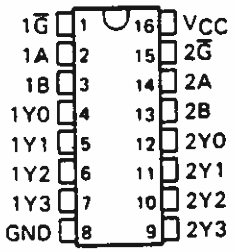
All of these decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design. The SN54LS139A and SN54S139 are characterized for operation range of −55°C to 125°C. The SN74LS139A and SN74S139A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

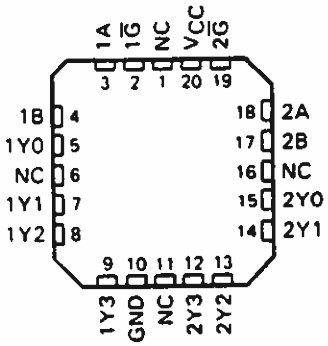
INPUTS			OUTPUTS			
ENABLE $\overline{G}$	SELECT B	SELECT A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

SN54LS139A, SN54S139 . . . J OR W PACKAGE
SN74LS139A, SN74S139A . . . D OR N PACKAGE
(TOP VIEW)

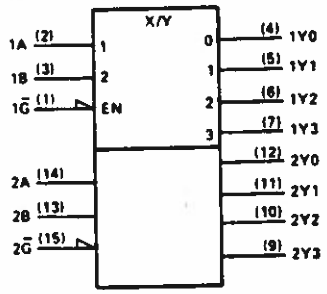


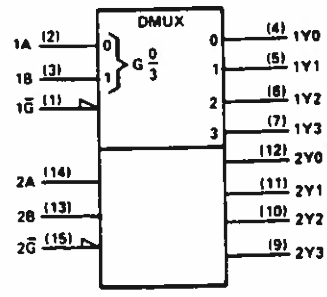
SN54LS139A, SN54S139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

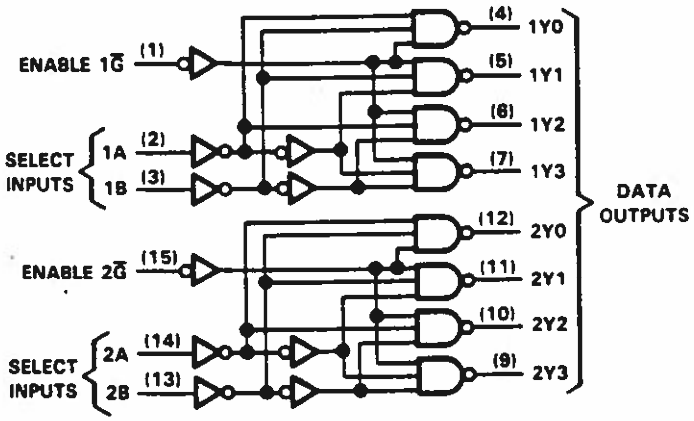
logic symbols (alternatives)†





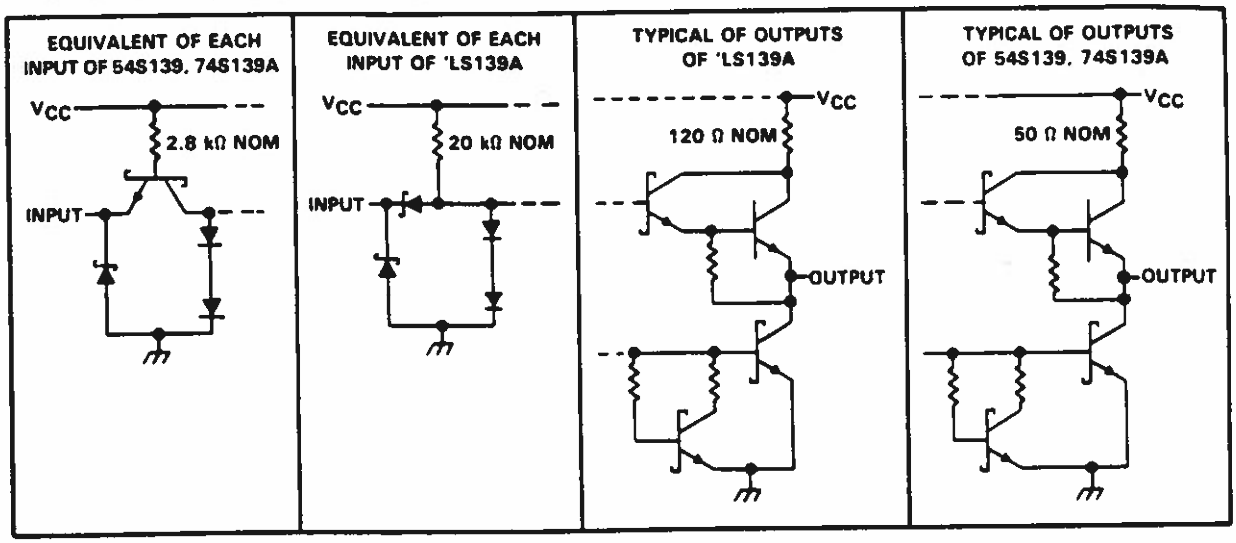
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage: 'LS139A . . . . . 7 V
54S139, 74S139A . . . . . 5.5 V
Operating free-air temperature range: SN54LS139A, SN54S139 . . . . . −55°C to 125°C
SN74LS139A, SN74S139A . . . . . 0° C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54LS139A			SN74LS139A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS139A			SN74LS139A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	V_{CC} = MAX, Outputs enabled and open			6.8	11		6.8	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 2)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54LS139A SN74LS139A			UNIT
					MIN	TYP	MAX	
t_{PLH}	Binary Select	Any	2	R_L = 2 kΩ, C_L = 15 pF		13	20	ns
t_{PHL}						22	33	ns
t_{PLH}			3			18	29	ns
t_{PHL}						25	38	ns
t_{PLH}	Enable	Any	2			16	24	ns
t_{PHL}						21	32	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54S139			SN74S139A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54S139 SN74S139A			UNIT
			MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
		SN74S'	2.7	3.4		
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}§	V_{CC} = MAX		−40		−100	mA
I_{CC}	V_{CC} = MAX, Outputs enabled and open			60	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 2)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54S139 SN74S139A			UNIT
					MIN	TYP	MAX	
t_{PLH}	Binary Select	Any	2	R_L = 280 Ω, C_L = 15 pF		5	7.5	ns
t_{PHL}						6.5	10	ns
t_{PLH}			3			7	12	ns
t_{PHL}						8	12	ns
t_{PLH}	Enable	Any	2			5	8	ns
t_{PHL}						6.5	10	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

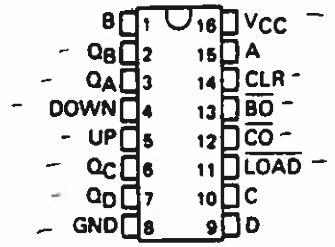
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

DECEMBER 1972—REVISED MARCH 1988

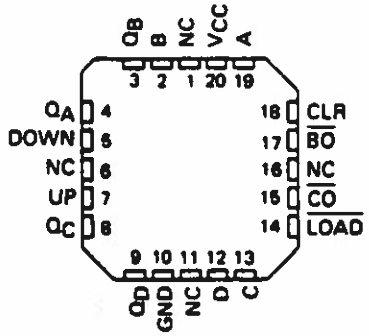
- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'LS192, 'LS193	32 MHz	95 mW

SN54192, SN54193, SN54LS192, SN54LS193 . . . J OR W PACKAGE
SN74192, SN74193 . . . N PACKAGE
SN74LS192, SN74LS193 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS192, SN54LS193 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192 and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

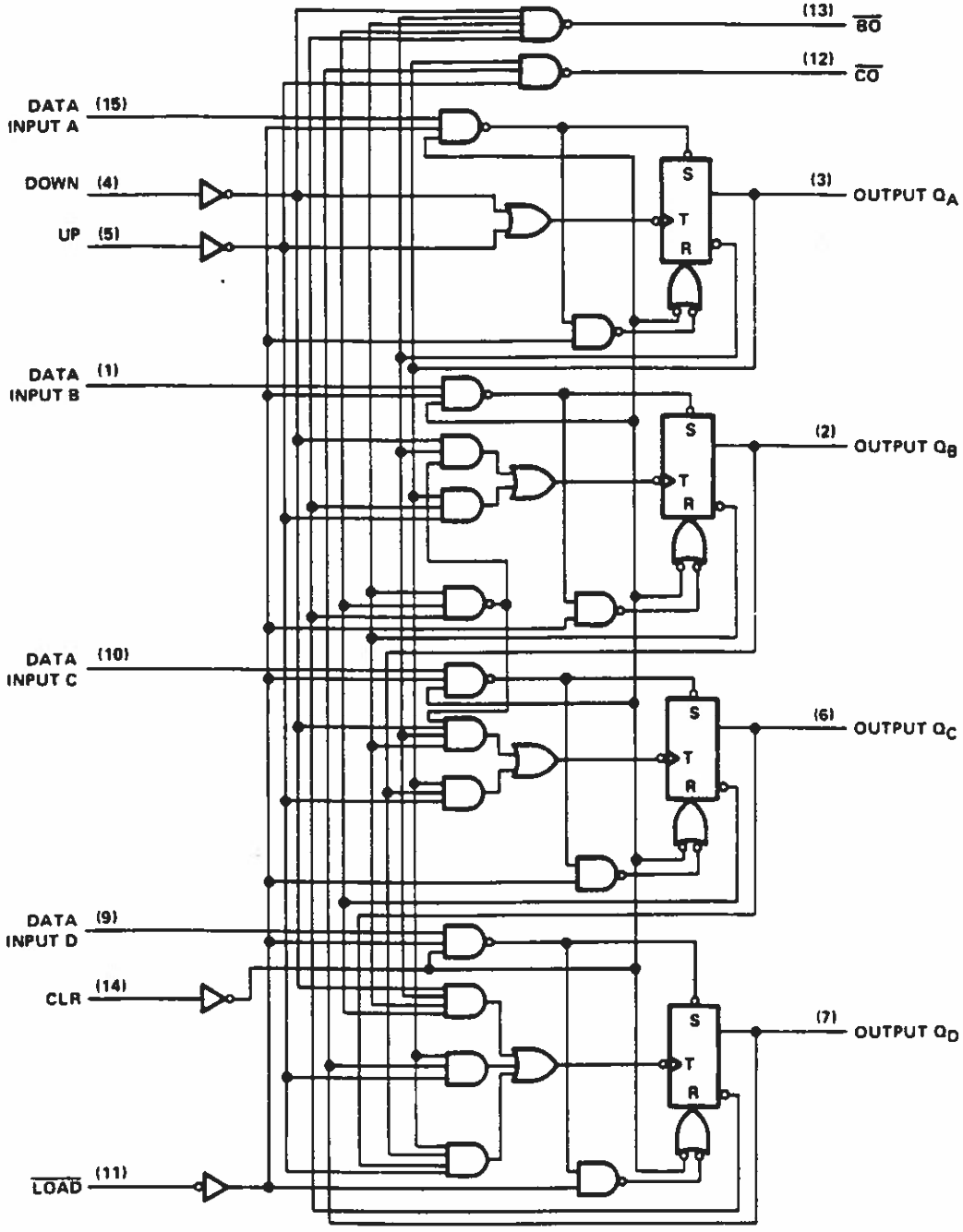
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storage temperature range	−65 to 150		−65 to 150		°C

NOTE 1: Voltage values are with respect to network ground terminal.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

TEXAS INSTRUMENTS
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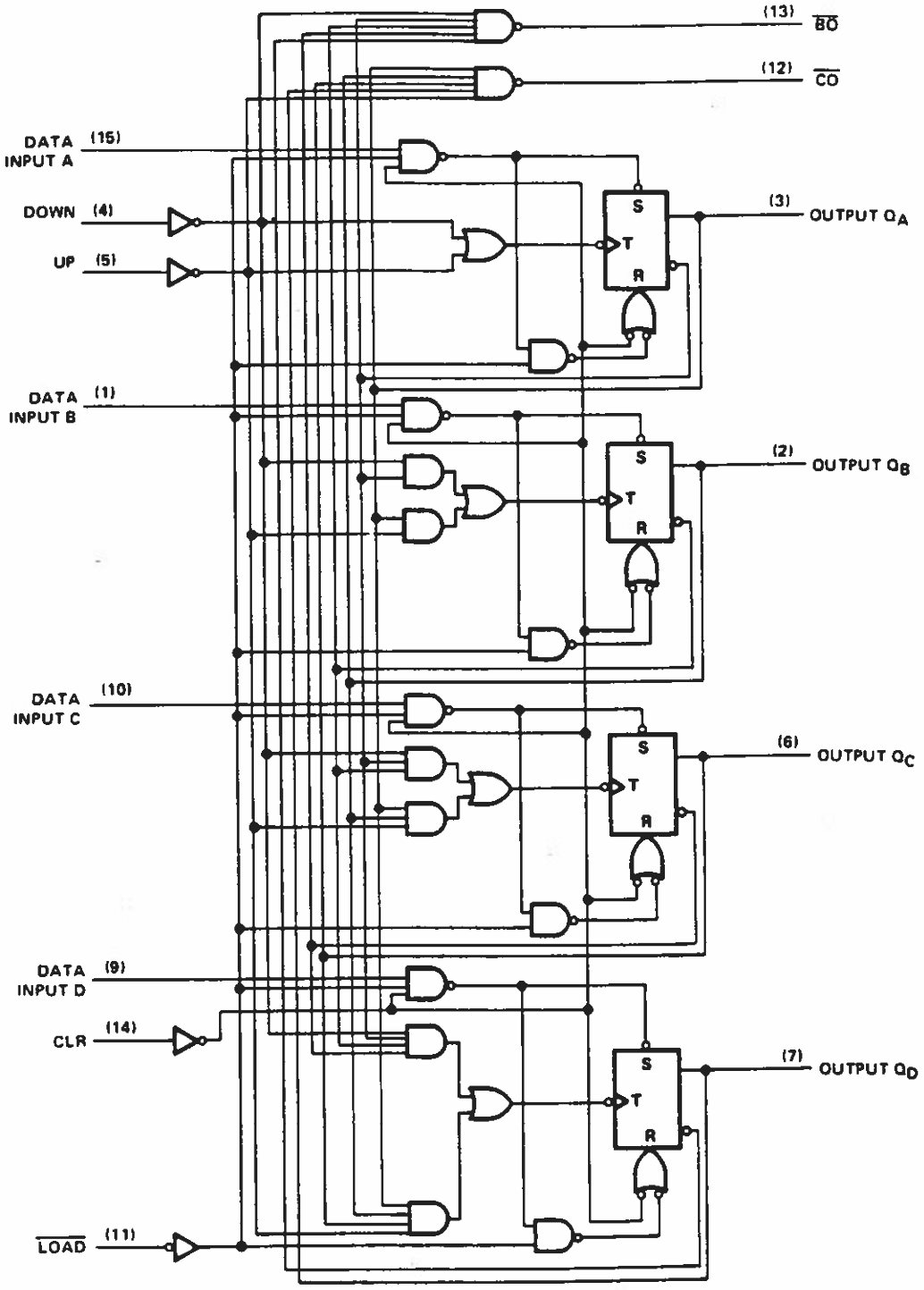
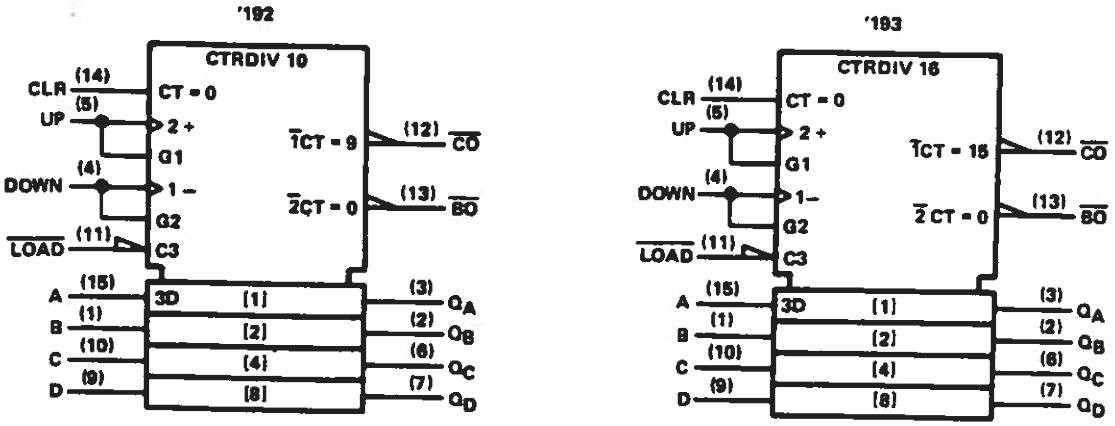
logic diagram (positive logic)



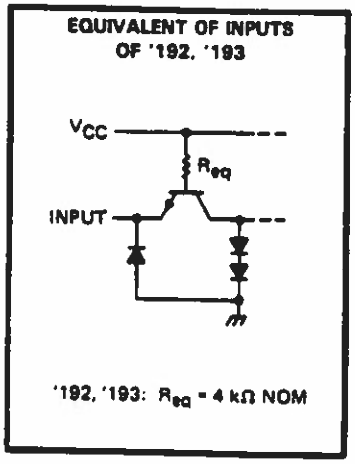
Pin numbers shown are for D, J, N, and W packages.

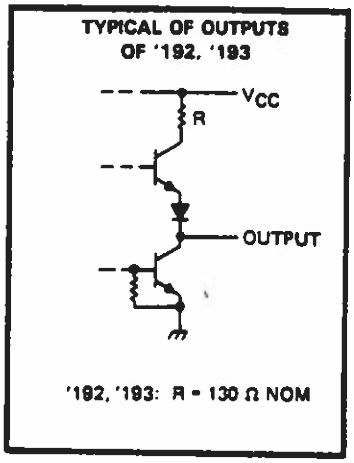
logic symbols†

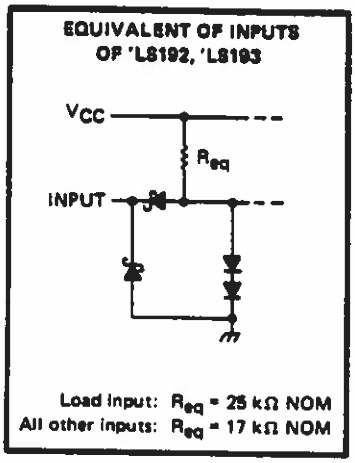


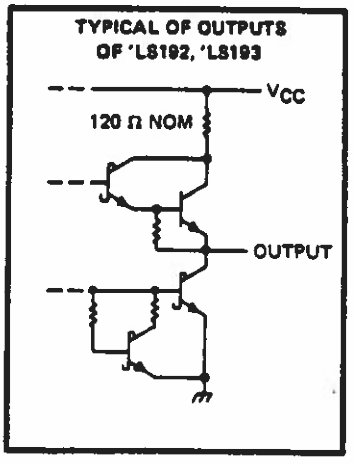
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs









TEXAS INSTRUMENTS
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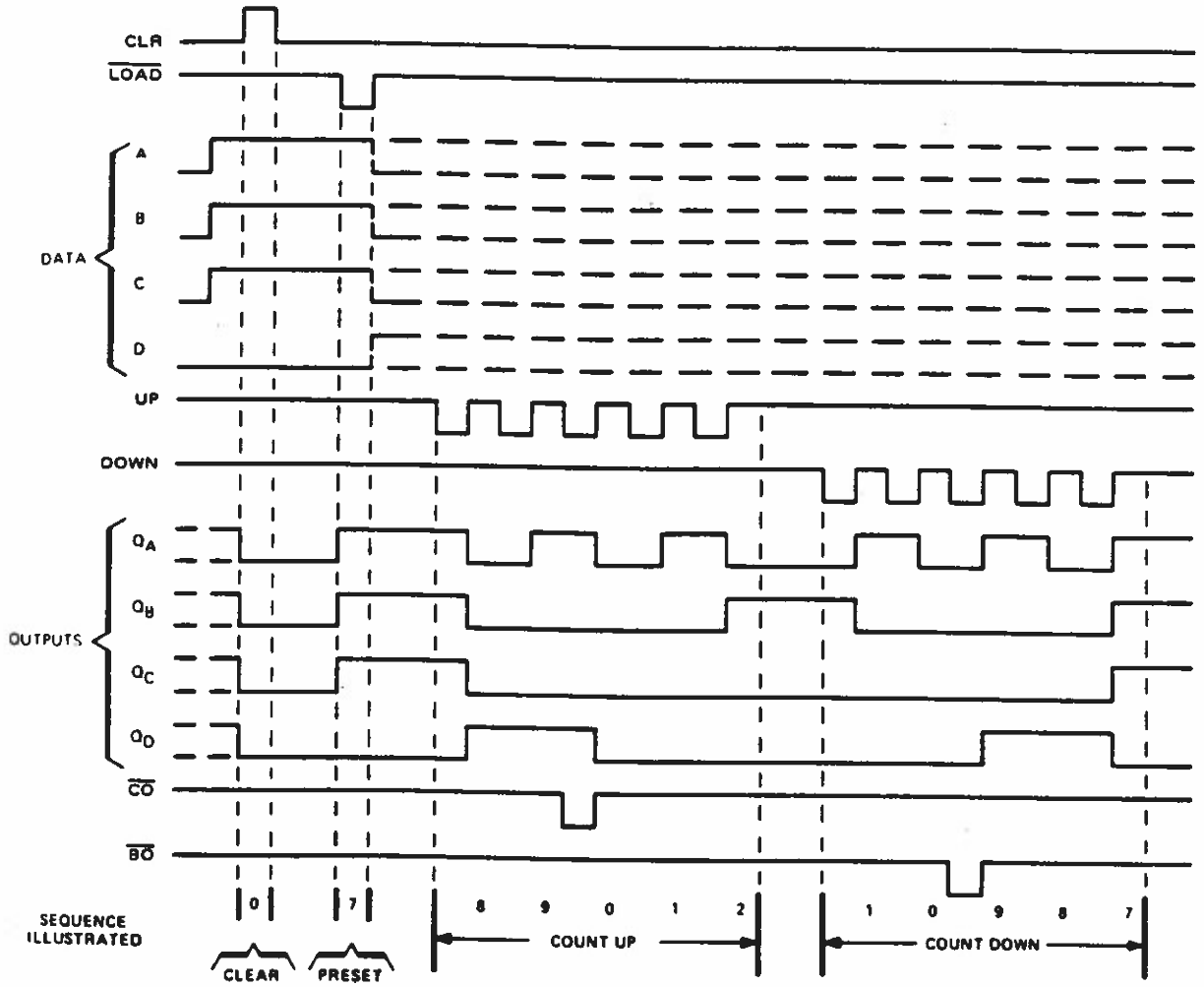
'192, 'LS192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



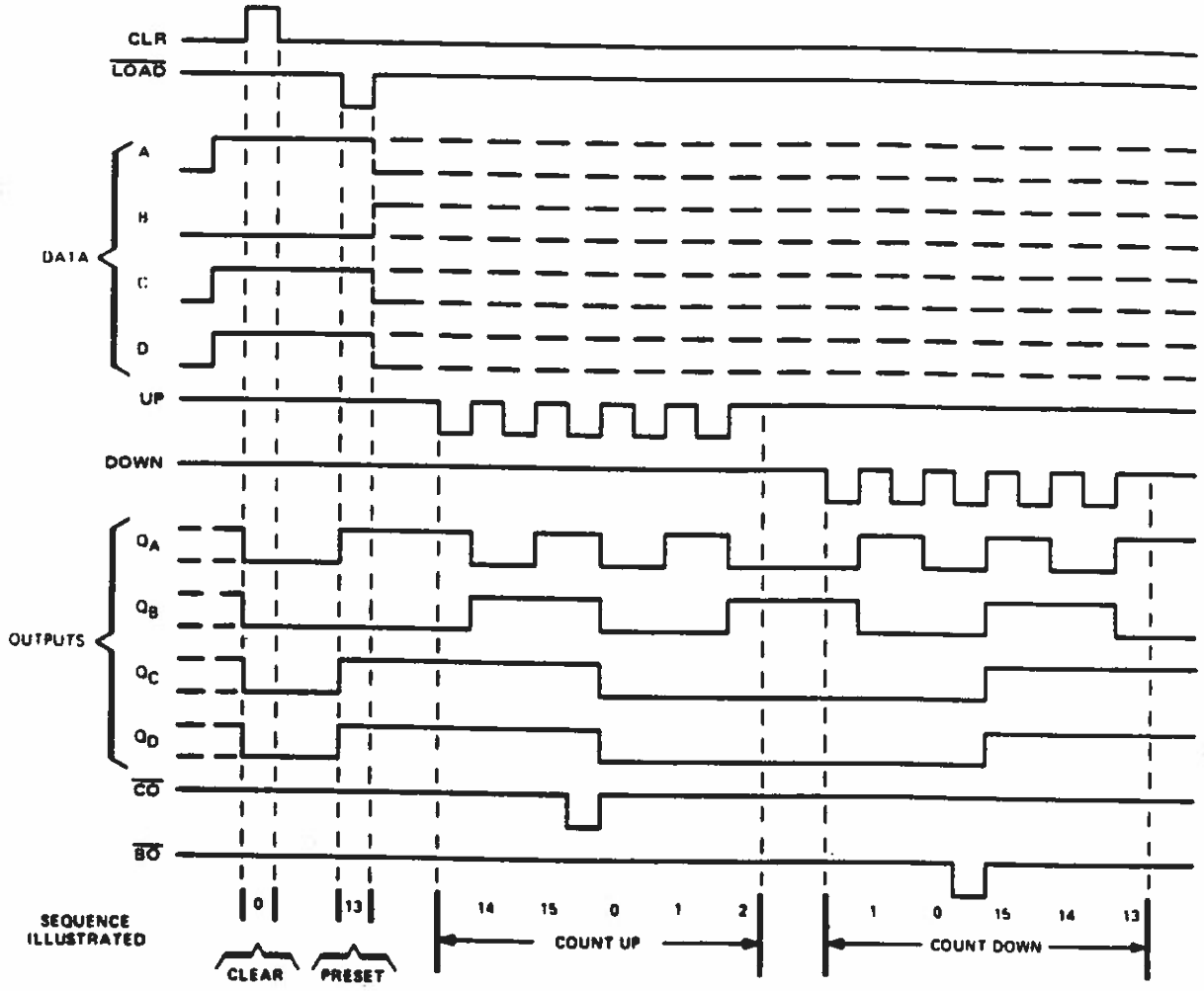
NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

'193, 'LS193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

TEXAS INSTRUMENTS
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Boolean Algebra

E-54 Digital Logic

a two-valued (binary) axiomatic system

0/1 ~ transistor off/on ~ voltage low/high..

- Basic operations $f(A, B)$

A	B	f_0	f_1	...	f_6	f_7	f_8	f_9	...	f_{14}	f_{15}
0	0	0	0		0	0	1	1		1	1
0	1	0	0	...	1	1	0	0	...	1	1
1	0	0	0		1	1	0	0		1	1
1	1	0	1		0	1	0	1		0	1
			AND		$\oplus$	OR	NOR	$\odot$		NAND	

NOT $\bar{A}$ — A A — $\bar{A}$

OR A, B — A+B NOR A, B — $\overline{A+B}$

AND A, B — AB NAND A, B — $\overline{AB}$

XOR A, B — $A \oplus B = A\bar{B} + \bar{A}B$ XNOR A, B — $A \odot B = \overline{A \oplus B} = AB + \bar{A}\bar{B}$

- constants: 0, 1
- variables: A, B, C, ...
- functions: $f(A, B, C) = (A + B \cdot 1) + C \cdot 0$

- axioms & theorems

$$A+0=A \qquad A\cdot 1=A$$
$$A+1=1 \qquad A\cdot 0=0$$
$$A+A=A \qquad A\cdot A=A$$
$$A+\bar{A}=1 \qquad A\cdot\bar{A}=0$$

- Commutative

$$A+B=B+A \qquad A\cdot B=B\cdot A$$

- Combinative

$$A+(B+C)=(A+B)+C \qquad A\cdot(B\cdot C)=(A\cdot B)\cdot C$$

- distributive

$$A+(BC)=(A+B)(A+C) \qquad A(B+C)=AB+AC$$

- De Morgan Law

$\bar{f}(A,B,\cdots)$ can be obtained by replacing $A, B, \cdots$ by $\bar{A}, \bar{B}, \cdots$
$\cdots$ $\bar{A}, \bar{B}, \cdots$ by A, B
$\cdots$ $+, \cdot$ by $\cdot, +$
$\cdots$ $0, 1$ by $1, 0$
in $f(A, B, \cdots)$.

- algebraic manipulation

EX $f(A,B)=A+\bar{A}B=A(B+\bar{B})+\bar{A}B$

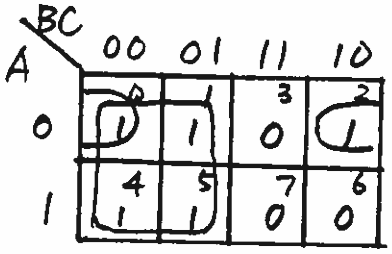
$=AB+A\bar{B}+AB+\bar{A}B$

$=A(B+\bar{B})+(A+\bar{A})B$

$=A\cdot 1+1\cdot B=A+B$

- Truth table & Karnaugh Maps

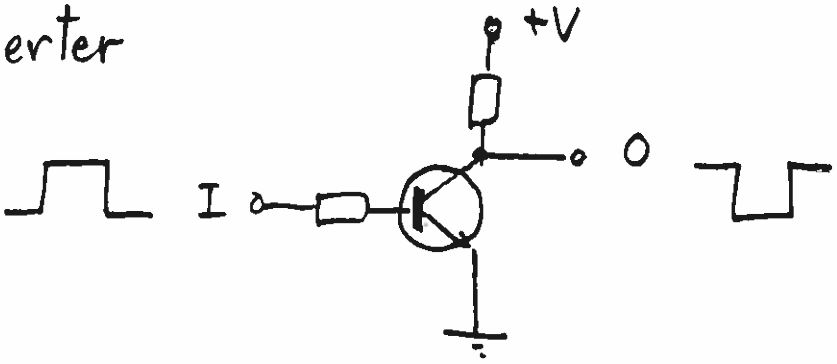
	A	B	C	f(A,B,C)
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	1	1	1	0



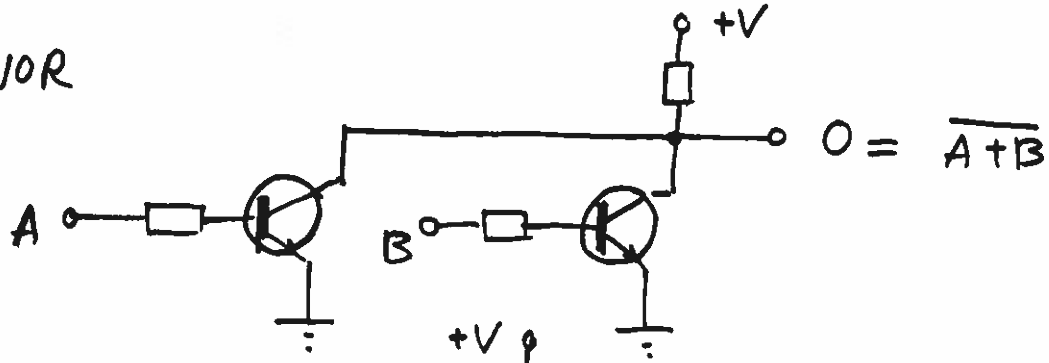
$f(A,B,C) = \bar{B} + \bar{A}\bar{C}$

Hardware Implementation

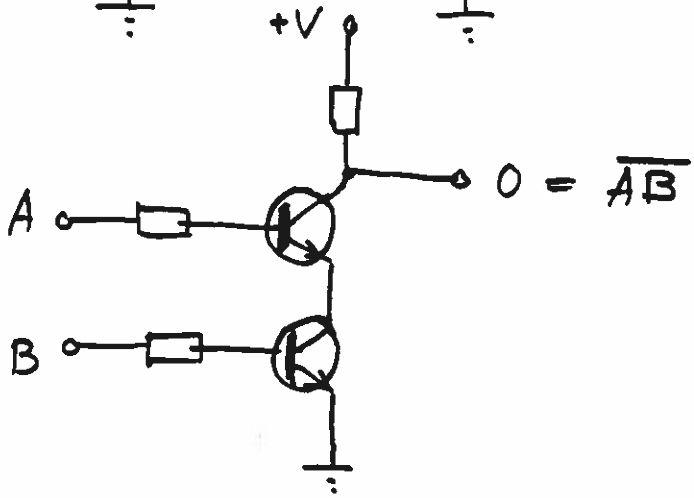
- inverter



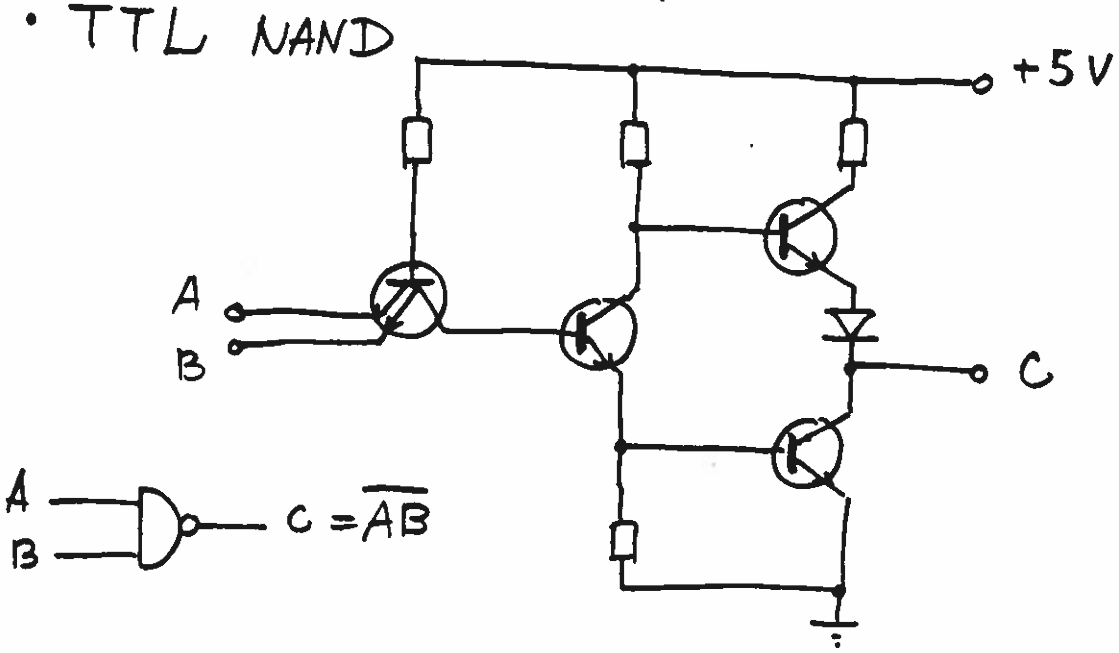
- NOR

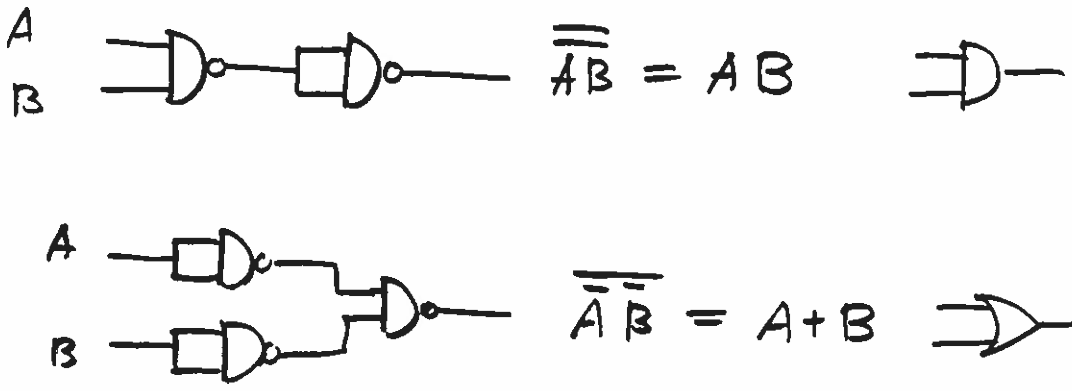


- NAND



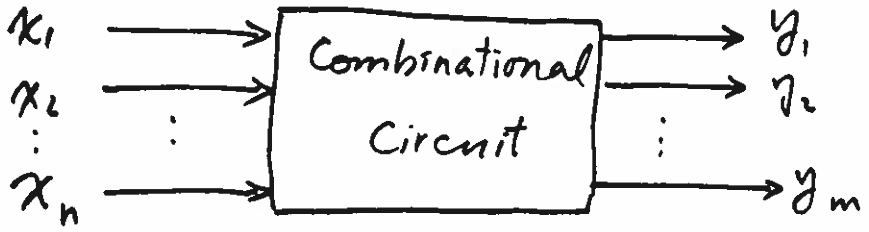
- TTL NAND




A
B
$\overline{\overline{A}\overline{B}} = AB$
A
B
$\overline{\overline{A}\overline{B}} = A+B$

Combinational Circuits

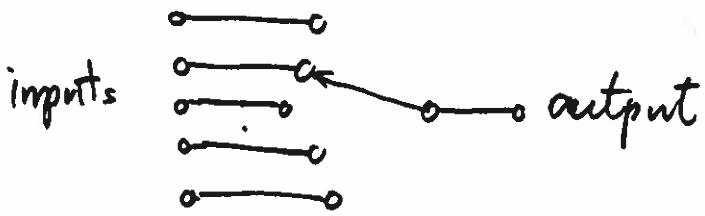
Connected arrangement of logic gates with a set of inputs and a set of outputs. At any given time, the outputs are a function of the combination of the inputs

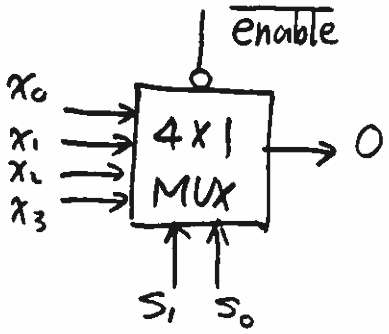


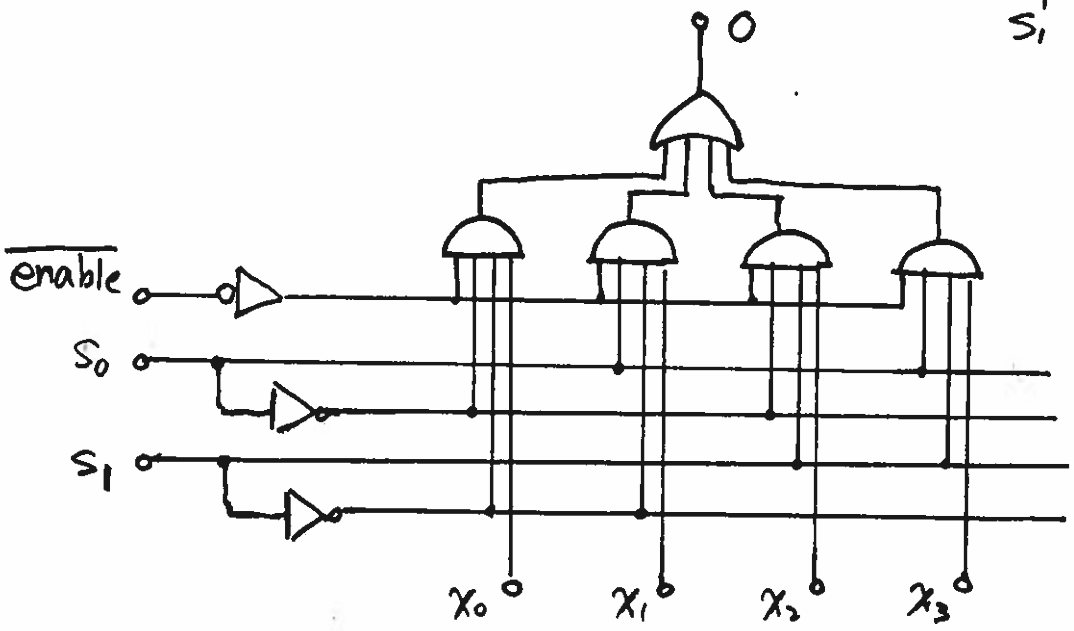
n inputs. 2^n combinations.

m outputs. $y_i = f_i(x_1 \cdots x_n)$ $i = 1, 2, \cdots m$

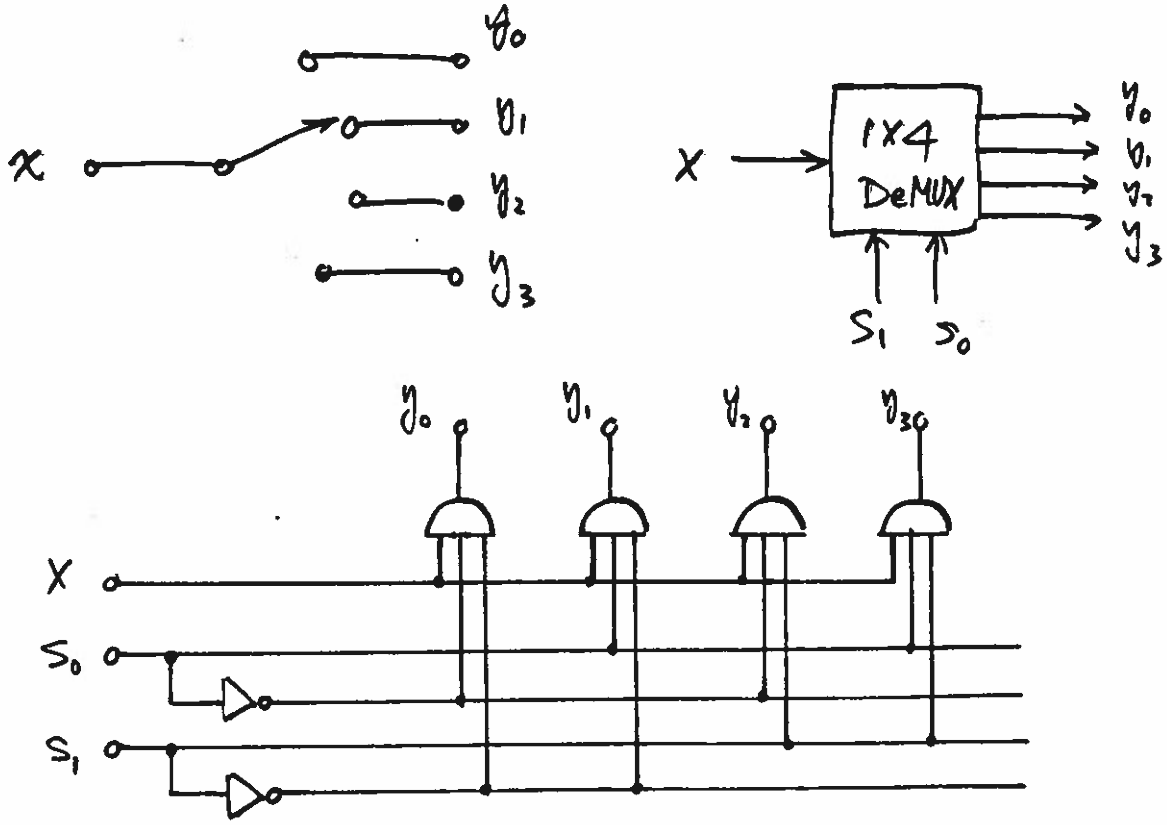
- Multiplexers MUXs



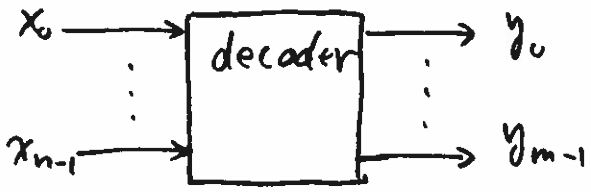




- De MUXs



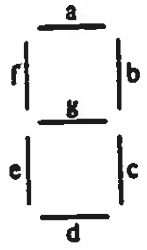
- Decoders convert binary information from one coded form into another



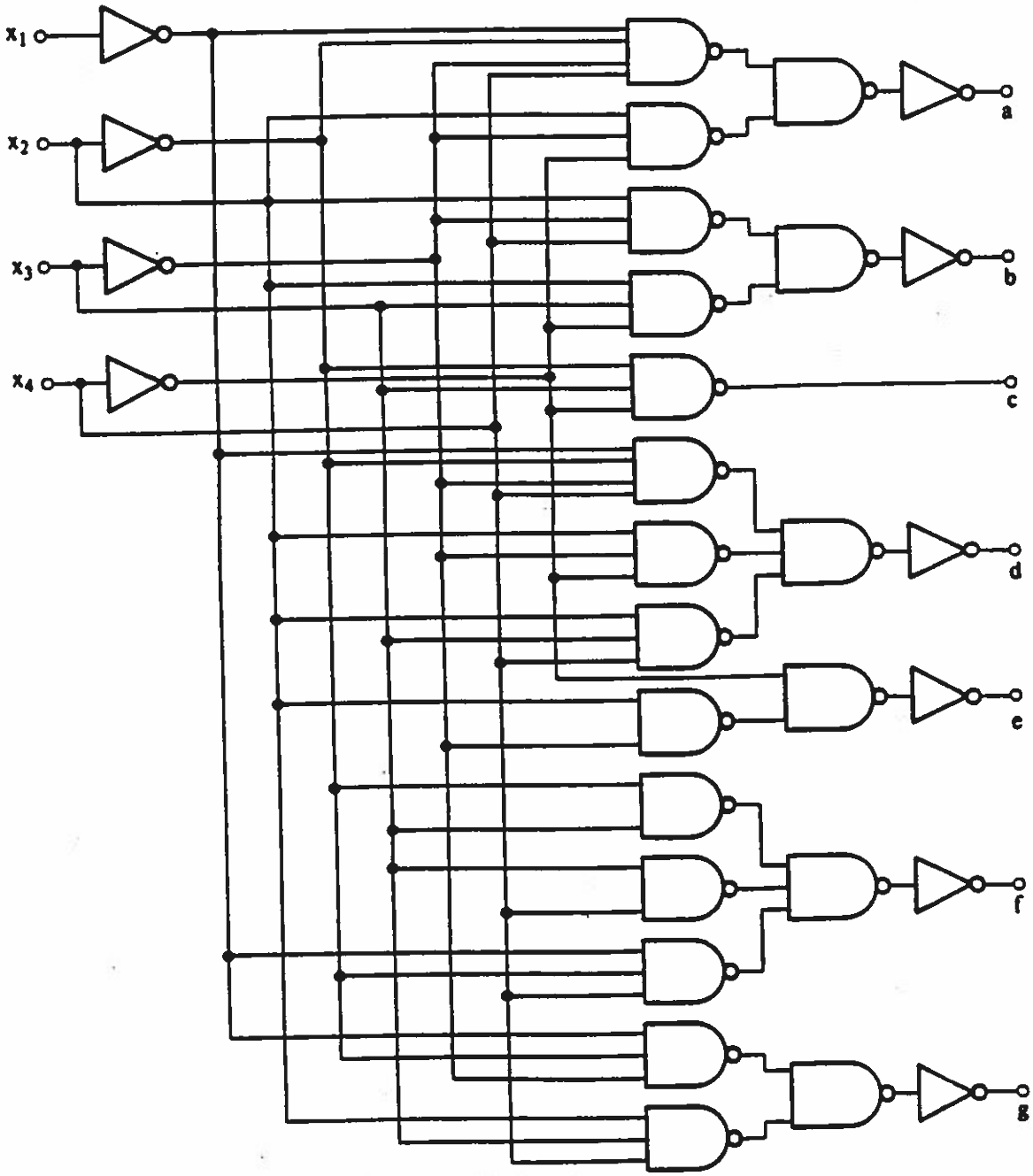
x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

EX 1: binary decoder = de MUX w/ $X \equiv 1$

EX 2: BCD (binary coded decimal) to 7-segment display decoder



No.	x_1	x_2	x_3	x_4	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

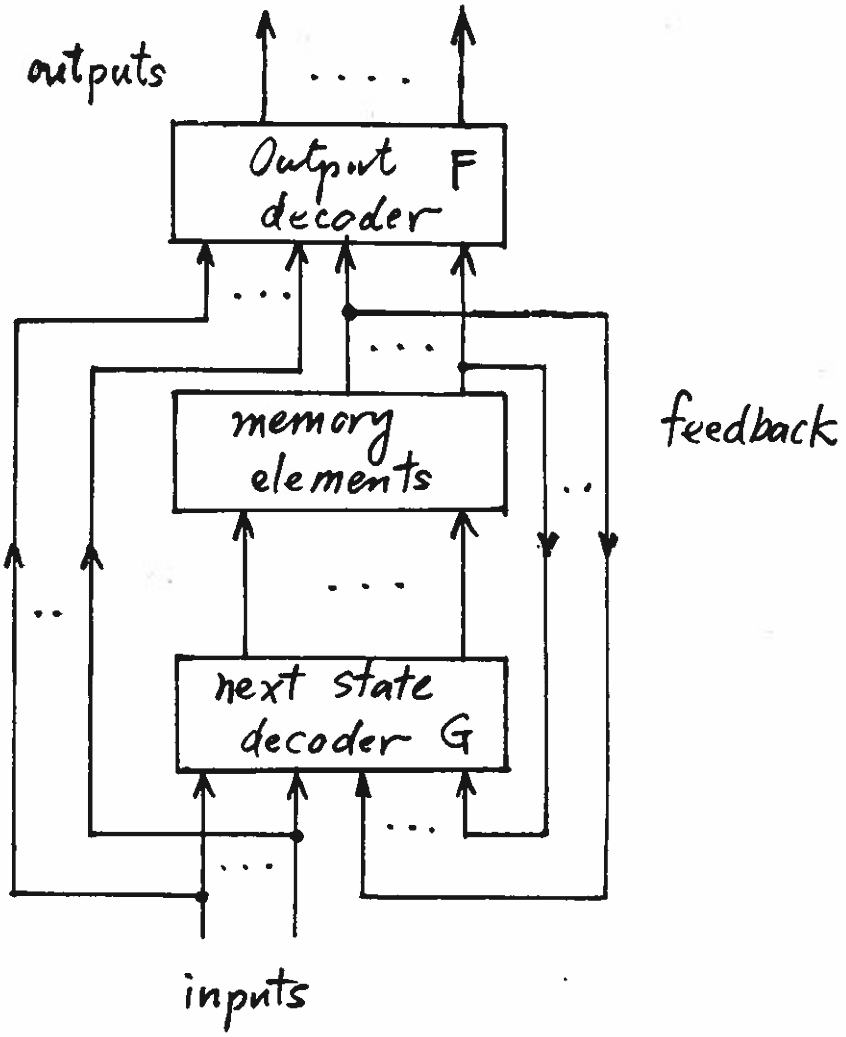


A BCD to seven-segment display decoder.

Sequential Circuits

the outputs of the circuit depend on the sequence of the inputs

- memory capability : memory elements
- feedback from memory elements to input

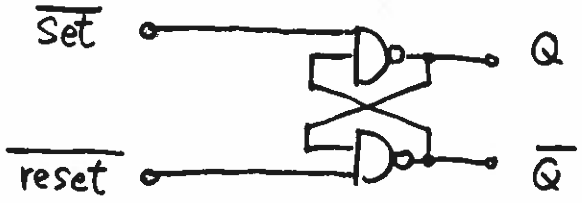


Output = F (Input, Current-state)

Next-state = G (Input, Current-state)

Memory Elements — Flip-Flops

- Basic Cell

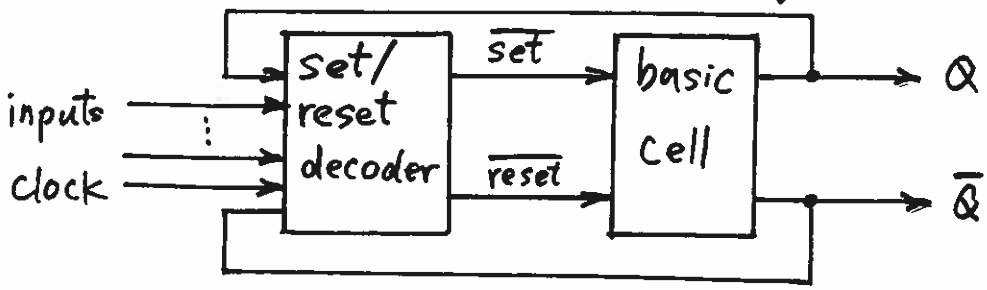


2 stable states:

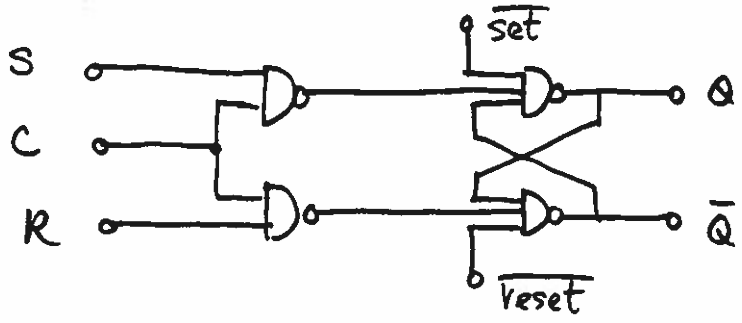
$Q=0 \quad \bar{Q}=1$

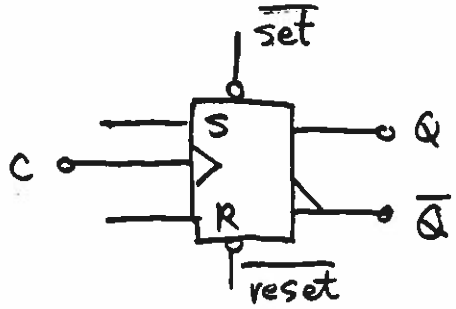
$Q=1 \quad \bar{Q}=0$

- clocked FFs (active only when clock is high)



- RS-FF (Set-reset)

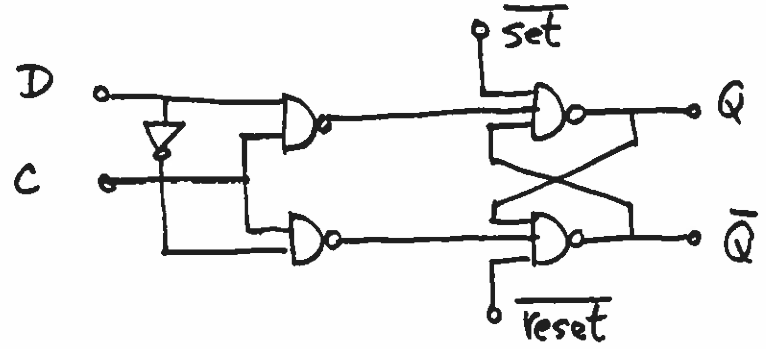


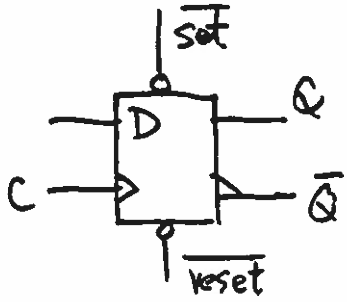


S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	not allowed

characteristic table

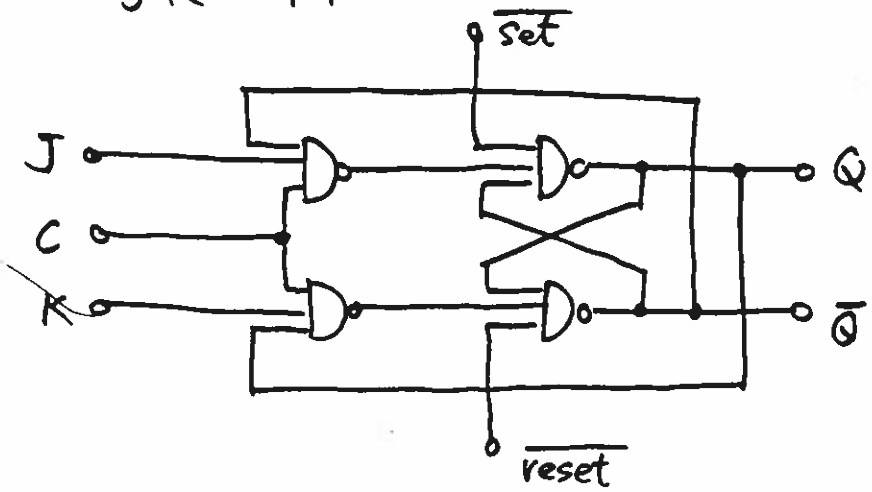
- D - FF (delay)

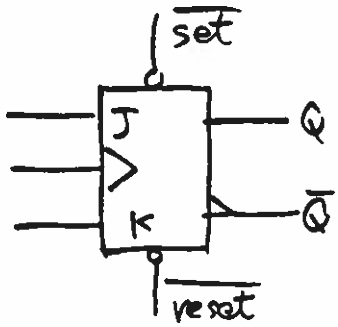




D	Q(t+1)
0	0
1	1

- JK - FF





J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\bar{Q}$(t)

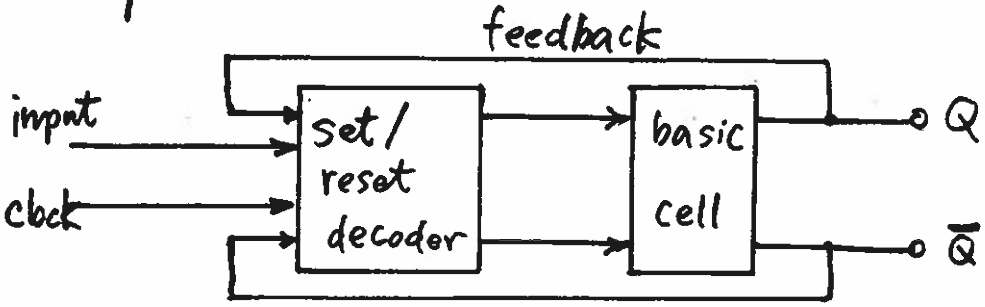
- T - FF (toggle)

tie J, K together

T	Q(t+1)
0	Q(t)
1	$\bar{Q}$(t)

Hardware Implementation

- two problems

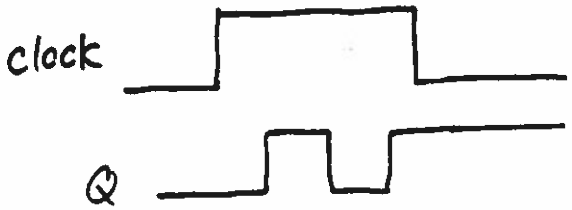


next-state = G(Input, current-state)

during active period (clock = high), any change in input or current-state (Q) will cause undesired state change.

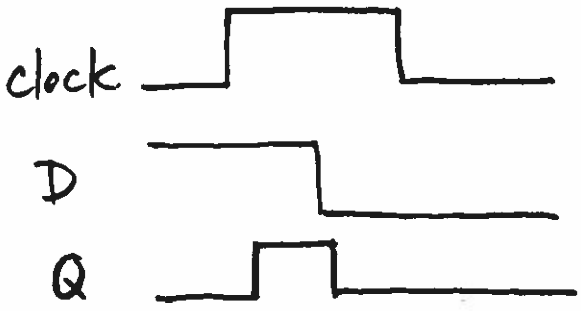
- Oscillation (caused by state change)

EX T-FF



- "Catch 0" or "catch 1" (caused by input change)

EX D-FF

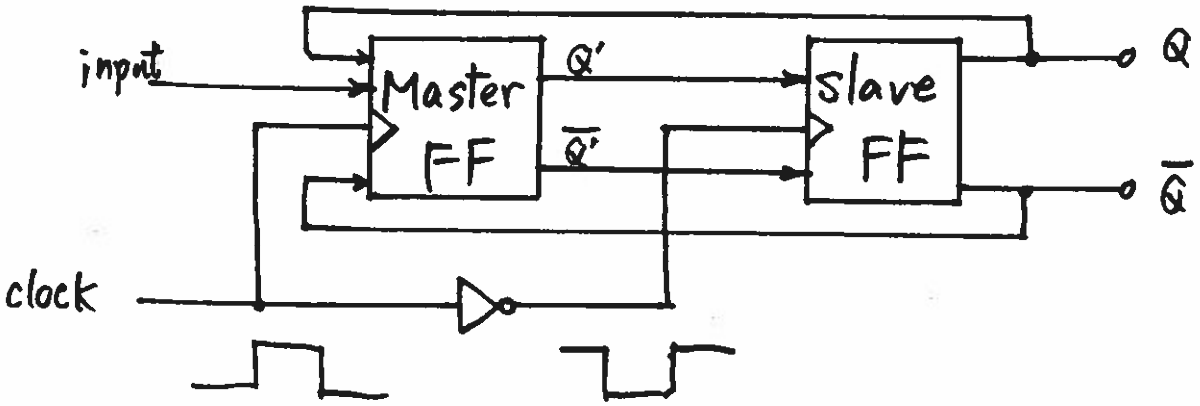


- solutions

  - narrow clock pulse

    high frequency interference. Not good

  - Master/Slave FF (MS FF)



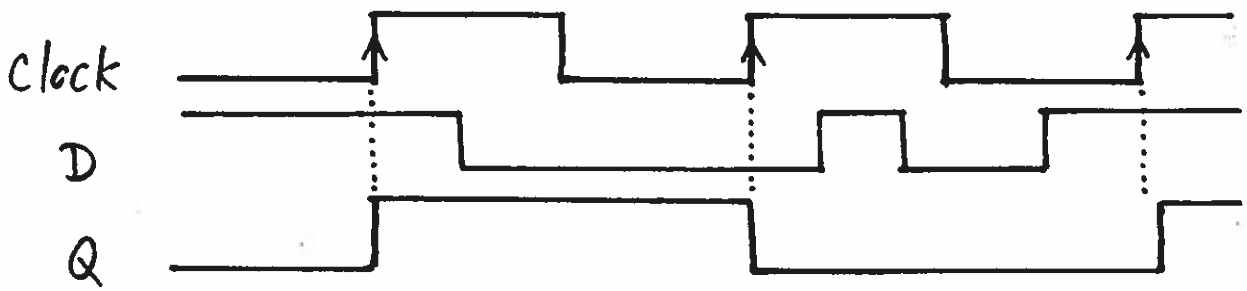
the oscillation problem caused by feedback is solved. but not "catch 0/1" problem caused by input change

  - Edge-triggered FF

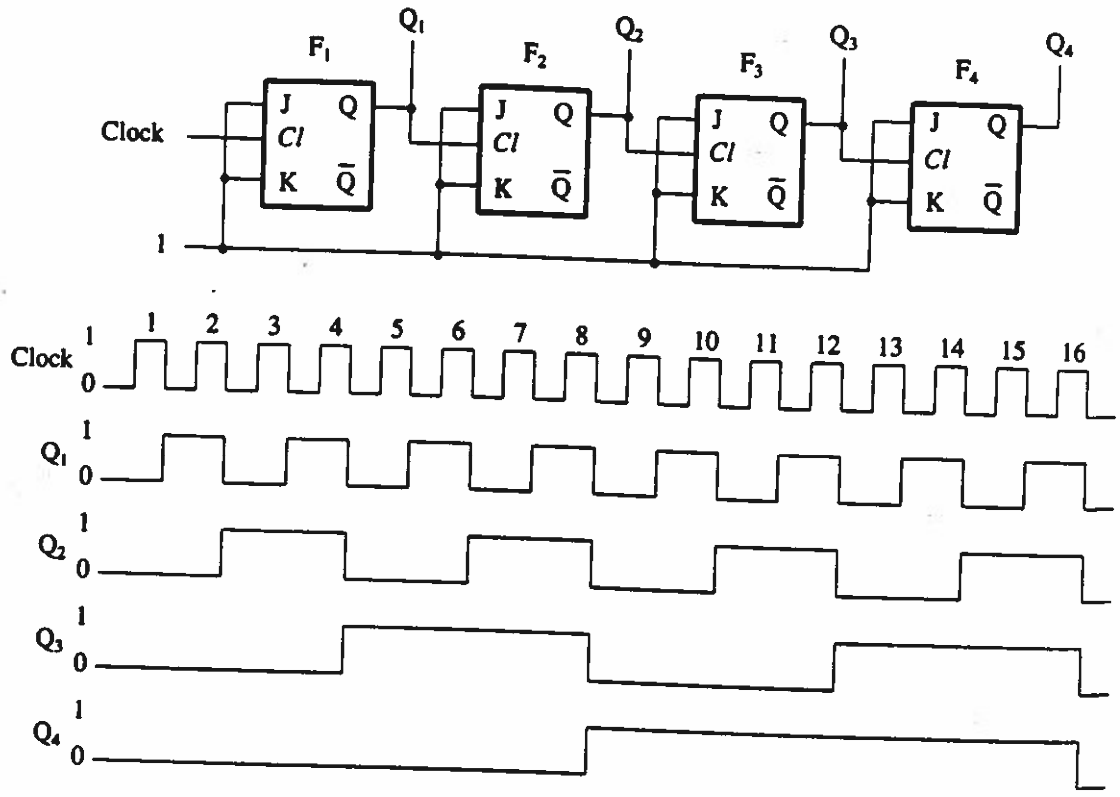
    only at the time instance of the rising (or trailing) edge of the clock, can the input/feedback affect the state.

    (sampling)

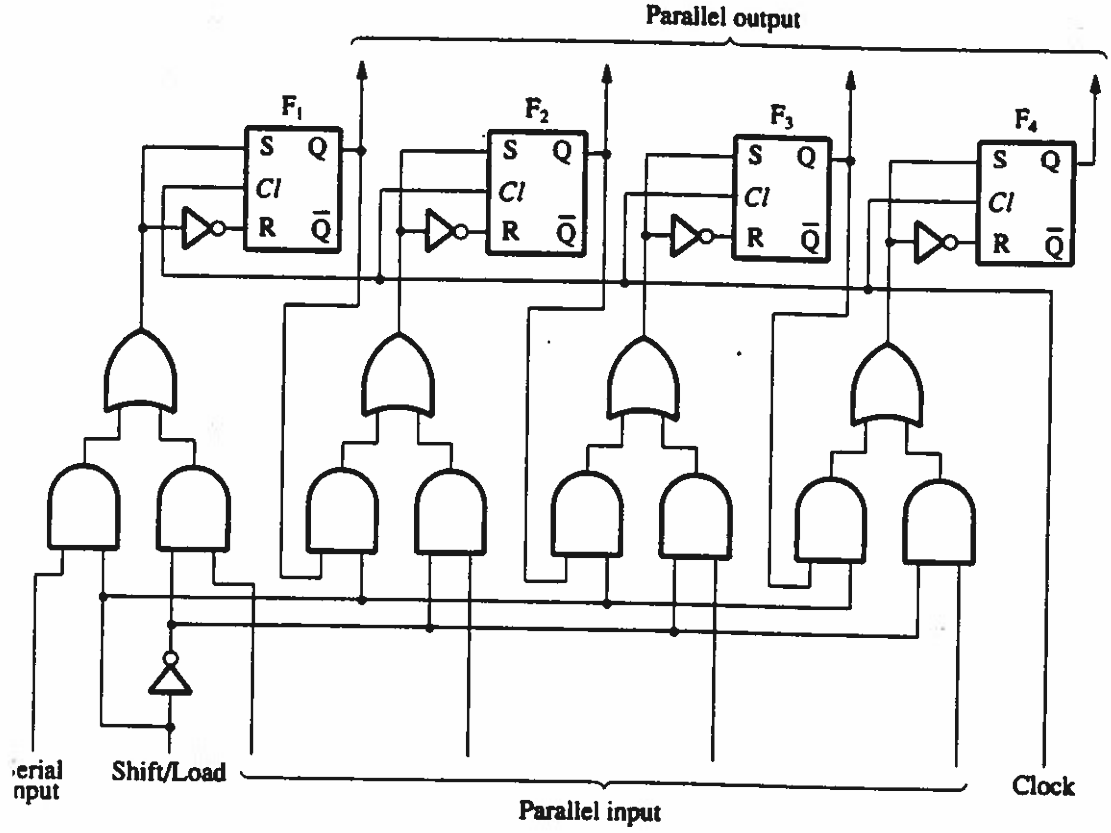
EX



- Binary Counter



- Shift/load Register



- UP/Down Counter